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# Modeling and Loss Analysis of Wide Bandgap Power Semiconductor Devices

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# MODELING AND LOSS ANALYSIS OF WIDE BANDGAP POWER SEMICONDUCTOR DEVICES

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# ABSTRACT

In recent times, the development of high power density and high efficiency power converters has become critical in power electronics applications like electric vehicles, aircrafts, electric ships and so on. High-switching-frequency and high-temperature operation are required to achieve this target. However, these requirements are exceeding the theoretical material-related limits of silicon (Si) based devices. The emerging wide bandgap power semiconductor technology is a promising solution to meet these requirements. Silicon Carbide (SiC) and Gallium Nitride (GaN) are the most promising among all wide bandgap semiconductor materials. SiC and GaN have almost a three times larger bandgap (about 3eV), compared with Si (about 1eV). The breakdown electric field of SiC and GaN is one order of magnitude higher than that of Si. The higher breakdown electric field enables the design of wide bandgap power devices with a thinner and higher doped voltage blocking layer. For unipolar power devices, this can yield a lower on-state voltage drop and conduction loss. For bipolar power devices, this can lead to a shorter switching time and lower switching loss. The high thermal conductivity of SiC, together with large bandgap, allows SiC-based devices to operate at temperatures exceeding 200$^{o}$C. All of these properties make wide bandgap semiconductor devices a promising alternative to Si-based devices.

The research work in this Ph.D dissertation can be broadly divided into two parts: the development of power device models, and the development of loss models for wide

bandgap power devices.

First, in order to characterize the switching performance of GaN High Electron Mobility Transistor (HEMT), a simple and accurate circuit-simulator compact model for a normally-off GaN HEMT device is developed. The model parameters can be easily extracted from static I-V characteristics and C-V characteristics. This model captures reverse channel conduction, which is a very important feature for circuit designers. A parameter extraction method is proposed. A double pulse test-bench is built to test the switching behavior of GaN HEMT. The accuracy of the proposed GaN HEMT model is validated under resistive and inductive switching conditions, and simulation results match well with experiments in terms of device switching waveforms.

Second, the static and switching characterizations of a SiC MOSFET's body diode are carried out. The static characterization of SiC MOSFET's body diode is done using a curve tracer and a double pulse test bench is built to characterize the inductive switching behavior of SiC MOSFET's body diode. The reverse recovery of SiC MOSFET's body diode is shown at different junction temperatures, forward conduction currents and current commutation slopes. In order to evaluate the performance of SiC MOSFET's body diode in different applications, an accurate physics-based diode model is introduced to perform simulations of SiC MOSFET's body diode. The validation of the body diode model is presented to prove the accuracy of the device model over a wide temperature range.

Third, an accurate analytical loss model that takes into account parasitic elements for power converters utilizing SiC MOSFETs and SiC Schottky diodes is proposed. A novel feature of this loss model is that it considers the PCB parasitic elements in the

circuits and the ringing loss. The switching process is analyzed in details, and the typical switching waveforms are given. The analytical results are compared with experimental results to verify the proposed analytical loss model.

Finally, a performance projection method and scalable loss model for SiC MOSFETs and SiC Schottky diodes are developed. To our knowledge, this is the first scalable loss model that provides performance projection capability for future SiC MOSFETs and SiC Schottky diodes. The parameters of these models are extracted from device datasheets by using a curve fitting method. Loss estimation of future SiC MOSFETs and SiC Schottky diodes can be performed based on the proposed scalable loss model.

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# LIST OF SYMBOLS

| | |
|---|---|
| $V_{sat}$ | Carrier saturation velocity in silicon carbide (cm/s) |
| $\varepsilon_{SiC}$ | Dielectric constant of silicon carbide (F/cm) |
| $\mu_n$ | Electron mobility ($cm^2/V \cdot s$) |
| $\mu_p$ | Hole mobility ($cm^2/V \cdot s$) |
| $A$ | Active area ($cm^2$) |
| $C_{gd}$ | Capacitance between gate and drain (F) |
| $C_{ds}$ | Capacitance between drain and source (F) |
| $C_{gs}$ | Capacitance between gate and source (F) |
| $I_{ds}$ | Drain current (A) |
| $I_F$ | Forward current of Schottky diode (A) |
| $k$ | Boltzmann's constant (eV/K) |
| $W_{N-}$ | Width of drift region (cm) |
| $L_D$ | Drain-to-source switching loop parasitic inductance (H) |
| $L_G$ | Gate-to-source switching loop parasitic gate inductance (H) |
| $L_S$ | MOSFET source-leg parasitic inductance (H) |
| $N_{N-}$, $N_D$ | Doping concentration of drift region ($cm^{-3}$) |
| $q$ | Fundamental electronic charge (C) |
| $R_g$ | Gate resistance (Ω) |

| | |
|---|---|
| $K_{p1}$ | Forward conduction device constant for GaN HEMT ($A/V^2$) |
| $K_{p2}$ | Reverse conduction device constant for GaN HEMT ($A/V^2$) |
| $R_{on,sp}$ | Specific on-resistance ($\Omega \cdot cm^2$) |
| $\lambda_1$ | Channel length modulation coefficient for GaN HEMT (A/V) |
| $V_{th1}$ | Forward gate-source threshold voltage for GaN HEMT (V) |
| $V_{th2}$ | Reverse gate-source threshold voltage for GaN HEMT (V) |
| $T$ | Absolute temperature (K) |
| $V_{bi}$ | Built-in voltage in gate source junction (V) |
| $V_{BD}$ | Breakdown voltage (V) |
| $PB_1$ | Built-in potential for gate-drain capacitance (V) |
| $PB_2$ | Built-in potential for drain-source capacitance (V) |
| $m_1$ | Junction grading coefficient for gate-drain capacitance |
| $m_2$ | Junction grading coefficient for drain-source capacitance |
| $V_{diode}$ | Voltage across Schottky diode (V) |
| $V_{ds}$ | Voltage applied to drain and source (V) |
| $V_{gs}$ | Voltage applied to gate and source (V) |
| $V_{gd}$ | Voltage applied to gate and drain (V) |
| $D$ | Ambipolar diffusion coefficient ($cm^2/s$) |
| $\tau$ | High-level carrier lifetime (s) |
| $h_p, h_n$ | Recombination parameters ($cm^4/s$) |
| $J$ | Maximum current density ($A/cm^2$) |
| $g_{fs}$ | SiC MOSFET transconductance (A/V) |

| | |
|---|---|
| $C_L$ | Load inductor equivalent parallel capacitance (F) |
| $C_{d1}$ | SiC Schottky diode junction capacitance (F) |
| $L_s$ | Main switching loop parasitic inductance (nH) |
| $L_{s2}$ | Common source parasitic inductance (nH) |
| $Q_{gd}$ | Miller charge for SiC MOSFET (C) |
| $R_{th(J-C)}$ | Thermal resistance between junction and case (K/W) |
| $C_{r0}$ | Zero-voltage-bias junction capacitance of SiC Schottky diode (F) |
| $T_j$ | Junction temperature of power device ($^o$C) |

# CHAPTER 1

# INTRODUCTION

## 1.1 WIDE BANDGAP SEMICONDUCTOR DEVICES FOR POWER ELECTRONICS

Power electronics can be defined as the application of solid-state electronics to condition, control and convert electric power. With increasing concern for energy delivery and environmental protection, power electronics is playing an increasingly important role in human society. Power semiconductor devices are the core solid-state components in the overall power conversion system, and they most often incur the largest portion of power losses in that system. Therefore, the development of power semiconductor devices has been the driving force in the progress of power electronics systems. Until recently, silicon (Si)-based devices have dominated the power device market due to mature and well-established fabrication technology for Si. However, with the growing need for high temperature, high power density and high frequency operation, silicon devices are reaching some inherent limits in their performance. For example, a variety of applications in the aircraft, automotive, and energy exploration industries require power conversion systems to operate at an ambient temperature significantly above 200 °C, far beyond Si material limits. Consequently, a new generation of so-called wide bandgap semiconductor devices has emerged as viable replacements for the current Si-based power devices.

At present, silicon carbide (SiC) and gallium nitride (GaN) are the most promising among all wide band-gap semiconductor materials [1][2][3]. Table 1.1 compares the material properties of Si, SiC and GaN. SiC and GaN have approximately three times larger bandgap (about 3 eV) compared with Si (about 1 eV). A large bandgap results in lower leakage currents than Si, and consequently in a much higher operating temperature. The breakdown electric field of SiC and GaN is one order of magnitude higher than that of Si. The higher breakdown electric field allows the design of wide bandgap power devices with thinner and more highly-doped voltage-blocking layers. As a consequence, a lower on-state voltage drop and conduction loss for a given breakdown voltage can be achieved. The high thermal conductivity of SiC, together with the large bandgap, allows SiC-based devices to operate at temperatures easily exceeding 200 °C [4][5][6]. All of the above properties make wide bandgap semiconductor devices a promising alternative to Si-based devices.

Table 1.1 Physical characteristics of Si, SiC and GaN

| **Material Property** | **Si** | **SiC** | **GaN** |
|---|---|---|---|
| Bandgap (eV) | 1.1 | 3.2 | 3.4 |
| Critical Electric Field (MV/cm) | 0.3 | 3.2 | 3.5 |
| Electron Mobility ($cm^2/V \cdot sec$) | 1450 | 700 | 2000 |
| Electron Saturation Velocity ($10^6$ cm/sec) | 10 | 20 | 25 |
| Thermal Conductivity (W/m·K) | 130 | 700 | 110 |

### 1.1.1 Overview of Commercially Available SiC Power Devices

A substantial amount of research and development activity has occurred over the past 20 years in the development of SiC power devices. As a result, high voltage (from 600V to 1200V) SiC unipolar power switches, such as JFETs and MOSFETs have become commercially available on the market since 2011 from Cree, Infineon and other

manufacturers [7]. Compared to conventional Si-based devices with the same voltage ratings, these SiC active power devices offer much lower on-state resistance per unit area than Si MOSFETs and much faster switching speed than Si IGBTs and GTOs. The advantages of SiC also encouraged the commercialization of SiC Schottky diodes with blocking voltages from 600 V up to 1200V by Cree, GeneSiC and other device manufacturers. These SiC Schottky diodes provide ulta-fast switching speed and almost zero reverse recovery, compared with conventional Si p-i-n diodes. Fig 1.1 shows the main SiC device manufacturers and their relevant SiC power devices (note that SemiSouth has been out of business since 2013).

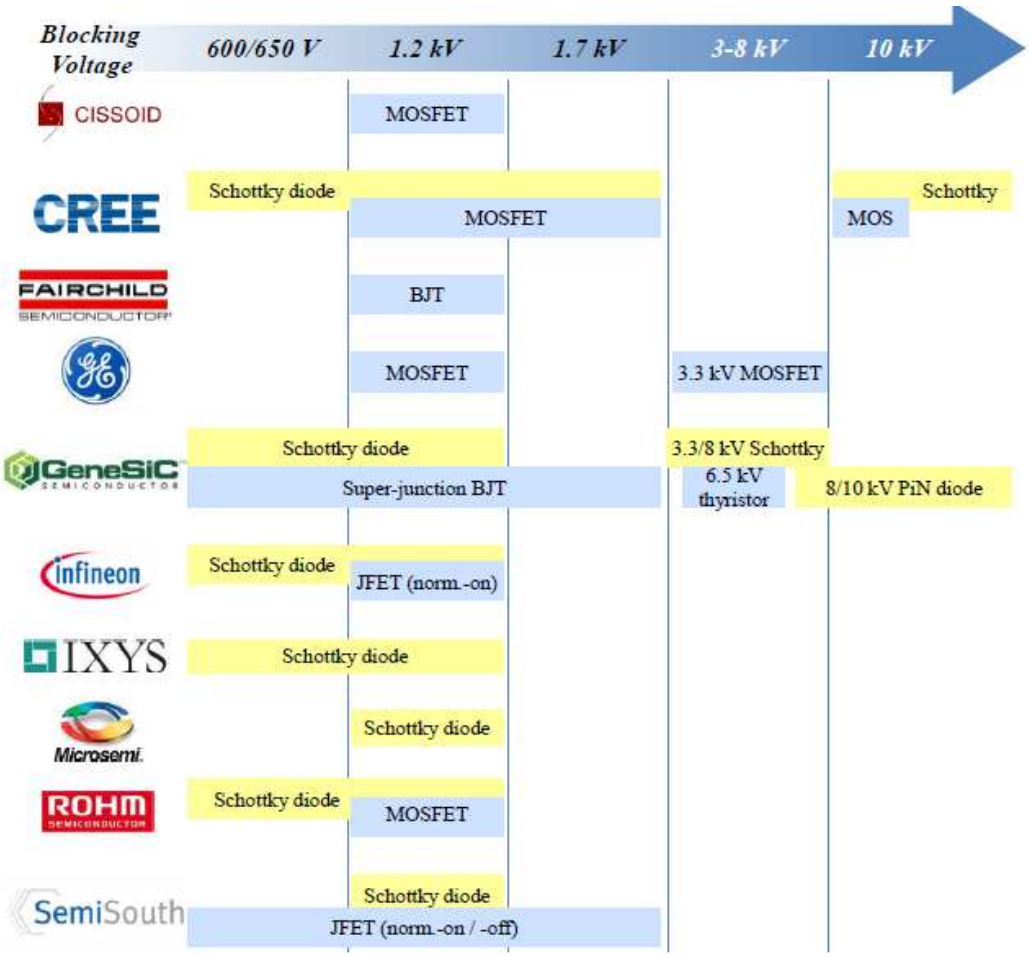



Figure 1.1 Major SiC power device manufacturers and their relevant products [8]

### 1.1.2 Overview of Commercially Available GaN Power Devices

Although GaN-based devices can theoretically offer better performance than SiC, the lack of good-quality substrates hinders the development of high-voltage vertical GaN power devices. However, the interest in GaN power devices by industry is increasing. At present, two types of GaN power devices have been reported: 1) GaN high-electron mobility transistors (HEMTs) and 2) GaN Schottky diodes. Currently, due to the lack of high quality GaN substrates, GaN epilayers are grown on substrates made of other materials, such as Si, SiC and sapphire. Silicon substrates are widely used for GaN-based devices, due to their low cost and mature fabrication techniques, even if the GaN epilayer quality is poor due to lattice mismatch. This lattice mismatch might introduce defects and lower device reliability. However, GaN substrates are becoming available, and they are expected to improve the resulting material quality and device performance.

Fig 1.2 shows the typical GaN HEMT lateral structure with three terminal contacts (source, gate and drain). A thick undoped GaN layer is grown on the Si substrate. On the top of the undoped GaN layer, an aluminum GaN (AlGaN) layer is grown. The conductivity of GaN HEMT is based on its piezoelectric property. A 2-D electron gas (2-DEG) is generated at the interface between AlGaN and GaN, with very high electron mobility (1200-2000$cm^2$/V s) and high conductivity [9].

Several GaN HEMT products having blocking voltages ranging from 30V to 650V have been released by various manufacturers, such as EPC, GaN Systems and Transphorm. The first commercially available discrete GaN HEMTs are from Efficient Power Conversion (EPC), and they are enhancement-mode devices. The enhancement-

mode GaN device is in the off state for zero $V_{gs}$ applied voltage, while a positive $V_{gs}$ is needed to turn it on. Presently, enhancement-mode GaN HEMTs from EPC have blocking voltages ranging from 30V to 450V. GaN Systems offers 100V and 650V enhancement-mode GaN HEMTs. Transphorm produces depletion-mode GaN transistors with 600V rating. A depletion-mode device is naturally conductive if no voltage is applied between gate and source. To turn off the device, a negative gate-source voltage is applied so that the 2-DEG under the gate is depleted. The cascode structure shown in Fig 1.3 is used with a depletion-mode GaN device to make the whole device operate like a normally-off device. In the cascode structure, a low-voltage silicon MOSFET is connected in series with the depletion-mode high-voltage GaN HEMT and the HEMT gate is connected to the MOSFET source. The low-voltage Si MOSFET controls the ON/OFF status of the high-voltage GaN HEMT [11][12][13].

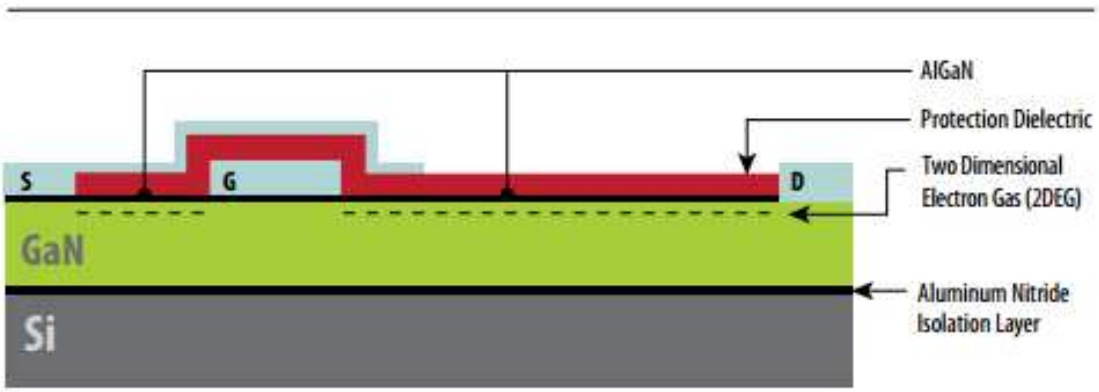



Figure 1.2 GaN HEMT structure [10]

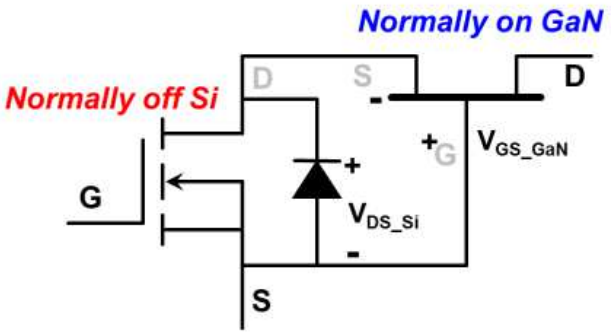



Figure 1.3 Cascode structure for depletion-mode GaN HEMT

Significant efforts have been made on high-voltage GaN Schottky diodes for high-frequency high-power switching applications [14]. Due to the lack of high-conductivity GaN substrates, most of the reported GaN Schottky diodes are based on the lateral structure. To my knowledge, no commercial GaN Schottky diode is currently available on the market.

## 1.2 Research Motivations and Objectives

The analysis and applications of wide bandgap power devices require a significant research effort, including the development of device models for wide bandgap power devices, and loss modeling of wide bandgap power devices. This dissertation describes contributions in three areas:

1. Development of wide bandgap power semiconductor device models
2. Development of analytical loss model for wide bandgap power devices
3. Development of performance projection method and scalable loss model for SiC MOSFETs and SiC Schottky diodes

### 1.2.1 Development of Wide Bandgap Power Semiconductor Device Models

Since power semiconductor device performance plays a key role in power electronics applications, power electronics designers need circuit-oriented device models to simulate the performance of power devices in different applications. The basic objective in device modeling is to obtain a predictive description of the current flow through the device as a function of the applied voltages and currents, environmental conditions, such as temperature and radiation, and physical characteristics, such as geometry, doping levels, and so on. In general, there is a trade-off between computational speed and model accuracy. The required accuracy and simulation time are crucial factors considered by device model designers when making this tradeoff. A very simple device model generally provides fast simulation speed, but does not provide physical insight into power device behavior and simulation accuracy is sacrificed. In contrast, a more complicated physics-based model is usually preferred for accurate simulation of device behavior, but it is very time-consuming and not very suitable for circuit simulations [15].

This dissertation focuses on the development of a simple and accurate circuit-simulator compact model for GaN HEMT, and a physics-based model for SiC MOSFET body diode.

### 1.2.2 Development of Analytical Loss Model for Wide Bandgap Power Devices

In power converter design, power losses of the power semiconductor devices are important because they strongly affect the efficiency of the power converter circuits and

determine the dimensioning of their cooling systems [16][17]. An accurate power loss model of the power semiconductor devices is needed for switching power converter design. Analytical loss models use closed form mathematical equations to accurately describe power loss mechanisms and quantify losses as a function of various design parameters. The efficiency and power loss can be estimated based on these analytical loss models.

In this project, my research focuses on analytical loss model development of SiC power semiconductor devices, such as SiC MOSFET and SiC Schottky diode. The proposed loss model should be able to accurately estimate the power losses, which are critical to evaluate the efficiency and physical size of power converters.

### 1.2.3 Development of Performance Projection Method and Scalable Loss Model for SiC MOSFETs and SiC Schottky Diodes

In 2011, Cree launched industry's first commercial SiC power MOSFET, which provided blocking voltage up to 1200V with an 80mΩ on-resistance at room temperature. Cree and other semiconductor manufacturers are also evaluating SiC power MOSFETs with higher blocking voltages (>1.2kV). However, higher-voltage SiC MOSFETs (>1.7kV) are not commercially available at the present time. Consequently no datasheet data is available and only limited sample device characterization has been published in the literature. In order to analyze the device behavior of upcoming high-voltage SiC MOSFETs (>1.7kV), power electronics researchers and engineers have a need for methods for future device performance projection.

The Schottky diode is also a very attractive unipolar device, formed by an electrically non-linear contact between a metal and a semiconductor bulk region. Cree has recently introduced its SiC Schottky diode products, with rated voltage ranging from 600V to 1700V, and rated current ranging from 1A to 100A. SiC Schottky diode is a very promising candidate to replace in the future silicon p-i-n diode for blocking voltage range from 600V to 3000V. Performance projection of SiC Schottky diodes for higher voltage and higher current ratings are also of interest for power electronics engineers.

Therefore, performance projection method and scalable loss model for SiC power devices are needed in system-level simulators like Smart Ship Systems Design (S3D) for power electronics researchers. S3D is a ship design tool that is capable of performing electric ship design concept development. It is critical to be able to project future SiC converter performance as the wide bandgap device technology advances. The objective of the proposed research is to produce models that accurately predict future SiC device performance. The proposed model will be able to answer system level questions such as converter efficiency, power dissipation, thermal cooling requirements and semiconductor temperature estimation.

## 1.3 State of The Art in Research

### 1.3.1 GaN HEMT Models

Power GaN devices have evolved rapidly in recent times. In particular, the GaN high-electron-mobility transistor (HEMT) is the most promising active device in GaN. GaN HEMT has a better Baliga figure of merit compared to state-of-the-art Si MOSFETs, because GaN HEMT has the features of low on-state resistance, small

parasitic device capacitance and high critical electric field [18]. As a result, GaN HEMT can switch at faster speeds and exhibit lower power loss. So far several device models have been proposed for GaN HEMT, most of them based on device physics. These physics-based device models provide more accuracy but have some disadvantages: they typically require several device parameters (which are usually unavailable to circuit designers) to apply the model to a specific device, they are complicated and require long simulation time [19]. Additionally, most of these models have originally been developed for RF or microwave applications, which are quite different from power electronics applications. Very few papers have been published on the development of device model for GaN HEMT in the power conversion area. In [20], a simple GaN power transistor model for DC-DC converters has been proposed, and it is shown to have good static characteristics in most respects. However, the paper does not provide switching characteristics and does not consider the reverse channel current conduction behavior of GaN HEMT. The reverse channel current conduction is of vital importance, because the GaN transistor has no body diode. When GaN HEMT is required to operate in the third quadrant, the reverse channel current conduction from source to drain functions as an equivalent body diode. In [21], a GaN HEMT model has been developed in SaberRD and static I-V and C-V characteristics have been validated, but the validation of switching characteristics is not provided.

### 1.3.2 SiC MOSFET Body Diode Models

In inductive hard switching, SiC MOSFET body diode is used if no external anti-parallel diode is connected. For example, in a synchronous buck converter the inductor current flows through the lower MOSFET body diode in a synchronous buck converter

during the dead time periods. In [22], the feasibility of using SiC MOSFETs in synchronous rectification is investigated. SiC MOSFET body diode shows less reverse recovery than Si MOSFET body diode, due to the shorter carrier lifetime in SiC material. In order to utilize the body diode of SiC MOSFET, a complete characterization (static and dynamic) of SiC MOSFET body diode is required. In addition, a circuit-oriented device model is needed to evaluate the performance of SiC MOSFET body diode in power converter design. However, only few papers investigate the characteristics of SiC MOSFET body diode and device model development of SiC MOSFET body diode.

A comparative performance study of Si and SiC MOSFET body diodes is conducted in [23]. The static and dynamic characteristics of Si and SiC MOSFET body diode are demonstrated. However, the characterization of SiC MOSFET body diode is not completed. For example, the temperature-dependent static characteristics of SiC MOSFET body diode are not available. In [24], the authors investigate the switching characteristics of SiC MOSFET body diode at varied temperatures, and switching loss from reverse recovery. In addition, in [25] the body diode turn-off behavior is characterized under different turn-off voltages, forward currents, current commutating slopes and junction temperatures.

In [26], A Fourier series method to model SiC MOSFET body diode is introduced. This model uses the Fourier series solution to the ambipolar diffusion equation. However, this model is not validated over a wide temperature range. The parameter extraction method for this model is not shown, which is crucial to the practicality of the model for the circuit designers.

### 1.3.3 Analytical Loss Model for SiC Power Devices

Power losses in power semiconductor devices consist of conduction loss and switching loss. The conduction loss can be accurately estimated from the device static I-V characteristics. The switching loss is dependent not only on device parameters, but also on circuit parameters, such as gate drive current, stray inductances and device parasitic capacitances. For switching loss estimation, the simplest analytical loss model treats power switch turn-on and turn-off current and voltage waveforms as piecewise linear. This conventional loss model yields closed form equations that can be easily used to calculate device switching loss. However, this model does not take into account parasitic elements from PCB layout and devices packages. Therefore, the loss prediction based on piecewise linear loss model is not accurate and does not match experimental results very well, especially for high frequency switching operation. In order to improve the accuracy of the analytical loss model, parasitic inductances in circuit and device capacitances should be considered.

Some papers have been published to propose analytical loss models for Si MOSFET. In [27] and [28], the effect of the nonlinearity characteristics of MOSFET capacitances is included in the proposed loss models. In addition, the parasitic inductances from PCB and device packages are also considered. The drawback of these models is their complexity. In [29], an analytical switching loss model is proposed for synchronous buck voltage regulators. The equations to calculate the rise and fall times are given. The impact of parasitic inductances is included in the model. However, the model is originally developed for low voltage Si MOSFETs, not for high voltage SiC MOSFETs. In addition, the MOSFET turn-off ringing loss is not included in the model.

### 1.3.4 Performance Projection Method and Scalable Model for SiC Power Devices

To my knowledge, no scalable loss model that provides performance projection capability for future SiC MOSFETs and SiC Schottky diodes can be found in the literature. A performance projection method and scalable loss model for future SiC power devices is a new research work in academia.

## 1.4 Contributions

There are four original contributions in this dissertation.

First, a simple and accurate circuit-simulator compact model for gallium nitride (GaN) high electron mobility transistor (HEMT) is proposed and validated under both static and switching conditions [30]. A novel feature of this model is that it is valid also in the third quadrant, which is important when the device operates as a freewheeling diode. The only measurements required for the parameter extraction are simple I-V static characteristics and C-V characteristics. A parameter extraction procedure is proposed. A double-pulse test-bench is built to characterize the resistive and inductive switching behavior of the GaN device. A simulation model is built in Pspice software tool, considering the parasitic elements associated with the PCB interconnections and other components (load resistor, load inductor and current shunt monitor). The Pspice simulation results are compared with experimental results. The comparison shows good agreement between simulation and experimental results under both resistive and inductive switching conditions. Operation in the third quadrant under inductive switching is also validated.

Second, the static and dynamic characterizations of SiC MOSFET body diode are presented. To my knowledge, this is the first complete characterization of SiC MOSFET body diode in literature. The static characterization of SiC MOSFET body diode is carried out using a curve tracer. The I-V curves of SiC MOSFET body diode at varied junction temperatures are given. The dynamic characteristics of SiC MOSFET body diode are tested based on a double pulse test bench. The switching behavior of SiC MOSFET body diode at different current commutating slopes, forward conduction currents and junction temperatures is demonstrated. The body diode device model is described in detail. A parameter extraction procedure is introduced to increase the practicality of the model for the circuit designers. The parameter extraction requires only data from the manufacturer's datasheets and one simple switching measurement. The body diode model is validated by experimental results over a wide temperature range.

Third, a simple and accurate analytical loss model for SiC power devices is developed. This model takes into account device capacitances and the parasitic inductances in the circuit, which is a very important feature for circuit designers. In addition, the ringing loss and the loss from reverse capacitive charging current of SiC Schottky diode are considered. The turn-on and turn-off transitions are analyzed in detail. The accuracy of the proposed model is validated by numerous experimental results, and the accuracy comparison of the proposed loss model and piecewise linear loss model is presented.

Finally, a performance projection method and a scalable loss model for SiC MOSFETs and SiC Schottky diodes are proposed [31]. To my knowledge, this is the first scalable loss model that provides performance projection capability for future SiC

MOSFETs and SiC Schottky diodes. The parameters of these models are extracted from device datasheets by using a curve fitting method. Loss estimation of future SiC MOSFETs and SiC Schottky diodes can be performed based on the proposed scalable loss model.

## 1.5 Dissertation Organization

Based on the above objectives, the dissertation is organized as follow:

Chapter 2 presents a simple and accurate circuit-simulator compact model for GaN HEMT. The static and switching characterizations on GaN HEMT are conducted. The only measurements required for the parameter extraction are simple I-V static characteristics and C-V characteristics. A parameter extraction procedure is proposed. The model for GaN HEMT is validated by numerous experiments over a wide temperature range.

In Chapter 3, the static and dynamic characterizations of SiC MOSFET's body diode are presented. The body diode device model is described in detail. A parameter extraction procedure is introduced to increase the practicality of the model for the circuit designers. Validation with experimental results demonstrates the accuracy of the body diode model.

Chapter 4 proposes a simple and accurate analytical loss model for SiC power devices. The turn-on and turn-off transitions are analyzed. The accuracy of the proposed model is validated by numerous experimental results, and the accuracy comparison of the proposed loss model and piecewise linear loss model is presented.

Chapter 5 develops a performance projection method and a scalable loss model for SiC MOSFETs and SiC Schottky diodes. The parameters of these models are

extracted from device datasheets by using a curve fitting method. Loss estimation of future SiC MOSFETs and SiC Schottky diodes can be performed based on the proposed scalable loss model.

Chapter 6 summaries the dissertation and gives some ideas for future work.

# CHAPTER 2

# CHARACTERIZATION AND MODELING OF A GALLIUM NITRIDE POWER HEMT

Gallium Nitride (GaN) is considered one of the most promising semiconductor material candidates for high-frequency, high-efficiency and high-power-density power conversion applications with significant advantages over silicon because of its excellent electrical properties, such as wider bandgap, higher thermal conductivity and higher critical breakdown electric field [32][33]. The GaN high-electron-mobility transistor (HEMT) is the most promising active device in GaN and is currently available from various manufacturers, such as EPC, International Rectifier, Transphorm, GaN Systems and others. GaN HEMT has a better Baliga figure of merit compared to state-of-the-art Si MOSFETs, because GaN HEMT exhibits low on-state resistance, small parasitic device capacitance and high critical electric field [34]. As a result, GaN HEMT can switch at faster speeds and exhibit lower conduction and switching losses [35][36][37]. Since power semiconductor device performance plays a key role in power electronics applications, power electronics designers need validated circuit-oriented device models to evaluate the performance of GaN HEMTs in different applications. The objective of this work is to develop a simple and accurate circuit-simulator compact device model, and validate it for commercially available GaN HEMT devices under static and switching conditions.

In this chapter, a simple and accurate circuit-simulator compact model for Gallium Nitride (GaN) high electron mobility transistor (HEMT) is proposed and validated under both static and switching conditions. A novel feature of this model is that it is valid also in the third quadrant, which is important when the device operates as a freewheeling diode. The only measurements required for the parameter extraction are simple I-V static characteristics and C-V characteristics. A detailed parameter extraction procedure is presented. Furthermore, a double-pulse test-bench is built to characterize the resistive and inductive switching behavior of the GaN device. A simulation model is built in Pspice software tool, considering the parasitic elements associated with the PCB interconnections and other components (load resistor, load inductor and current shunt monitor). The Pspice simulation results are compared with experimental results. The comparison shows good agreement between simulation and experimental results under both resistive and inductive switching conditions. Operation in the third quadrant under inductive switching is also validated.

## 2.1 Development of Device Simulation Model

The simple circuit-simulator compact GaN HEMT model developed in this work is shown in Fig 2.1. The model comprises a voltage-dependent current source $I_{ds}$, two voltage-dependent capacitances $C_{gd}$ and $C_{ds}$, a voltage-independent gate-source capacitance $C_{gs}$, and three parasitic resistances $R_g$, $R_s$ and $R_d$. The voltage-dependent current source $I_{ds}$ is used to model static current-voltage (I-V) characteristics for both forward and reverse conduction. The three parasitic capacitances play a vital role in determining device switching performance.

### 2.1.1 VOLTAGE-DEPENDENT CURRENT SOURCE $I_{DS}$

The voltage-dependent current source $I_{ds}$ is a bidirectional current source function of internal device node voltages $V_{ds}$ and $V_{gs}$. Since the device has a nearly symmetrical lateral structure, a positive gate-to-drain voltage will enhance channel conduction in the third quadrant in the same way as a positive gate-to-source voltage does in the first quadrant. Therefore, the forward and reverse channel conduction modes are both taken into account. In order to accurately predict power converter performance at different operating temperatures, accurate temperature-dependent device constant $K_p$ is used in the circuit model.

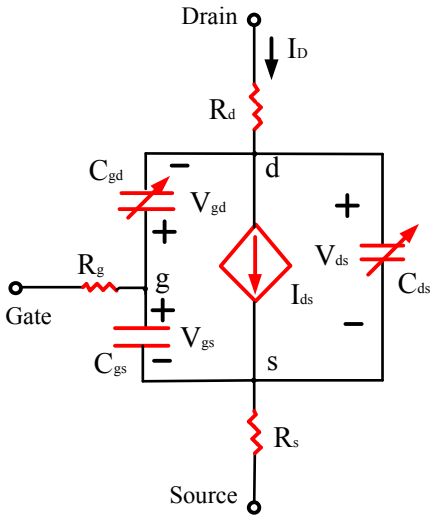



Figure 2.1 Structure of the GaN HEMT model

The model I-V characteristics are calculated using the following equations for the four operating modes: forward linear, forward saturation, reverse linear and reverse saturation mode.

1) Linear region in forward conduction mode ($V_{ds}>0$)

Operation in this region occurs when the gate-source voltage bias $V_{gs}$ is larger than the gate threshold voltage for forward channel conduction $V_{th1}$, and the internal node voltage bias $V_{ds}$ satisfies the equation

$$V_{ds} < V_{gs} - V_{th1} \qquad \text{Equation 2-1}$$

Under this condition, the current of the voltage-dependent current source is given by:

$$I_{ds} = K_{p1}\left[(V_{gs} - V_{th1})V_{ds} - V_{ds}^{2}/2\right] \qquad \text{Equation 2-2}$$

where $K_{p1}$ is the temperature-dependent device constant in forward conduction mode.

2) Saturation region in forward conduction mode ($V_{ds}>0$)

When the internal node voltage bias $V_{ds}$ satisfies the equation

$$V_{ds} > V_{gs} - V_{th1} \qquad \text{Equation 2-3}$$

the drain bias causes the device channel to pinch off at the drain end and the current is given by:

$$I_{ds} = K_{p1}(V_{gs} - V_{th1})^{2}(1 + \lambda_1 V_{ds})/2 \qquad \text{Equation 2-4}$$

where $\lambda_1$ is the channel length modulation parameter for forward channel conduction.

3) Linear region in reverse conduction mode ($V_{ds}<0$)

Whereas for forward conduction ($V_{ds}>0$) the voltage that controls channel conduction is the gate-source voltage $V_{gs}$, for reverse conduction ($V_{ds}<0$) the drain and source terminals reverse their roles and the controlling voltage is the gate-drain voltage $V_{gd}$. When the gate-drain voltage bias $V_{gd}$ is larger than the threshold voltage for reverse channel conduction $V_{th2}$, the channel current in this linear region is given by:

$$I_{ds} = -K_{p2}\left[(V_{gd} - V_{th2})V_{sd} - V_{sd}^2 / 2\right] \qquad \text{Equation 2-5}$$

where $K_{p2}$ is the temperature-dependent device constant in reverse conduction mode.

4) Saturation region in reverse conduction mode ($V_{ds}<0$)

When the voltage $V_{sd}$ satisfies the equation

$$V_{sd} > V_{gd} - V_{th2} \qquad \text{Equation 2-6}$$

the reverse conducting channel is pinched off at the source end and the current is given by

$$I_{ds} = -K_{p2}(V_{gd} - V_{th2})^2 / 2 \qquad \text{Equation 2-7}$$

5) Off region in both forward conduction and reverse conduction modes

For positive drain-source voltage, when $V_{gs}$ is smaller than threshold voltage $V_{th1}$, the channel in forward conduction is off and channel current $I_{ds}$ is equal to zero. Similarly, for negative drain-source voltage, when $V_{gd}$ is lower than threshold voltage $V_{th2}$, channel current $I_{ds}$ is also equal to zero, because the conduction channel is off in this case.

### 2.1.2 PARASITIC CAPACITANCES $C_{GS}$, $C_{GD}$ AND $C_{DS}$

Since gate-source capacitance is relatively independent of the voltage potentials applied to the electrodes, a constant gate-source capacitance $C_{gs}$ is used in this device model. This assumption is justified by device capacitance measurement shown in Fig 2.8.

Capacitances $C_{gd}$ and $C_{ds}$ are nonlinear voltage dependent parasitic capacitances, given by:

$$C_{gd} = \frac{C_{gd0}}{\left(1 + \frac{|V_{gd}|}{PB_1}\right)^{m_1}}$$ Equation 2-8

$$C_{ds} = \frac{C_{ds0}}{\left(1 + \frac{|V_{ds}|}{PB_2}\right)^{m_2}}$$ Equation 2-9

where $C_{gd0}$ is the zero-bias gate-to-drain capacitance, and $C_{ds0}$ is the zero-bias drain to source capacitance. $PB_1$ and $PB_2$ are the junction built-in potentials for gate-drain capacitance $C_{gd}$ and drain-source capacitance $C_{ds}$, respectively. The parameters $m_1$ and $m_2$ are the junction grading coefficients for gate-drain capacitance $C_{gd}$ and drain-source capacitance $C_{ds}$, respectively.

### 2.1.3 Parasitic Resistances $R_G$, $R_S$ and $R_D$

The internal gate resistance $R_g$ is assumed to be zero, compared with the external gate resistance typically introduced to dampen transient oscillations during switching transients. Resistances $R_d$ and $R_s$ are assumed to be constant and represent the distributed nature of terminal contact mesh.

### 2.1.4 Temperature Dependence of Device Constant $K_P$

In order to accurately estimate the device conduction loss versus temperature, the device model should include the temperature dependence of the device constant $K_p$,

which determines the voltage drop across the device as a function of current. A quadratic fit for the temperature dependence of the device constant $K_p$ is proposed:

$$K_p = K_{p0} / (1 + T_{c1}(T - T_0) + T_{c2}(T - T_0)^2) \qquad \text{Equation 2-10}$$

where $K_{p0}$ is the nominal device constant at room temperature, $T_0$ is nominal room temperature, and $T_{c1}$ and $T_{c2}$ are temperature coefficients.

The complete list of the needed parameters for the considered device model is shown in Table 2.1.

Table 2.1 GaN HEMT model parameters

| | |
|---|---|
| $K_{p1}$ | Forward conduction device constant at room temperature |
| $K_{p2}$ | Reverse conduction device constant at room temperature |
| $V_{th1}$ | Forward conduction threshold voltage |
| $V_{th2}$ | Reverse conduction threshold voltage |
| $\lambda_1$ | Forward conduction channel length modulation coefficient |
| $C_{gs}$ | Gate-source capacitance |
| $C_{gd0}$ | Zero-bias gate-drain capacitance |
| $PB_1$ | Built-in potential for gate-drain capacitance |
| $m_1$ | Junction grading coefficient for gate-drain capacitance |
| $C_{ds0}$ | Zero-bias drain-source capacitance |
| $PB_2$ | Built-in potential for drain-source capacitance |
| $m_2$ | Junction grading coefficient for drain-source capacitance |
| $R_d$ | Drain parasitic resistance |
| $R_s$ | Source parasitic resistance |
| $T_{c1\text{-}1}$ $T_{c2\text{-}1}$ | Temperature coefficients for forward conduction device constant |
| $T_{c1\text{-}2}$ $T_{c2\text{-}2}$ | Temperature coefficients for reverse conduction device constant |

## 2.2 Static Characterization and Parameter Extraction

The parameter extraction approach used in this model is based on static characterization of the semiconductor device. The device under investigation is the commercially available EPC 2001 (100V/25A) from EPC. Static I-V characteristics are measured with a Tektronix 371A curve tracer, and capacitance C-V characteristics with a Keithley 590 CV analyzer.

### 2.2.1 Static Characteristics of GaN HEMT

The forward output characteristic family of curves is measured under different gate-source voltage bias conditions (from 2V up to 5V) in Fig 2.2. The reverse output characteristic curves under different gate-source voltage bias conditions (from -3V up to 2V) are shown in Fig 2.3. It is interesting to notice that the reverse characteristic curves do not exhibit saturation characteristics similar to the forward characteristics curves. This is due to the fact that these characteristics are measured with a curve tracer under constant gate-source voltage $V_{gs}$=const, but for reverse conduction the controlling voltage is the gate-drain voltage $V_{gd}$. As source-drain voltage $V_{sd}$ increases, gate-drain voltage also increases according to

$$V_{gd} = V_{gs} + V_{sd} = const + V_{sd} \qquad \text{Equation 2-11}$$

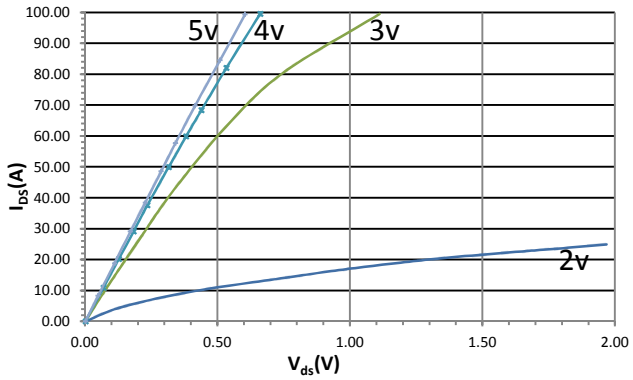



Figure 2.2 Measured forward output I-V characteristics at room temperature 25ºC for EPC2001

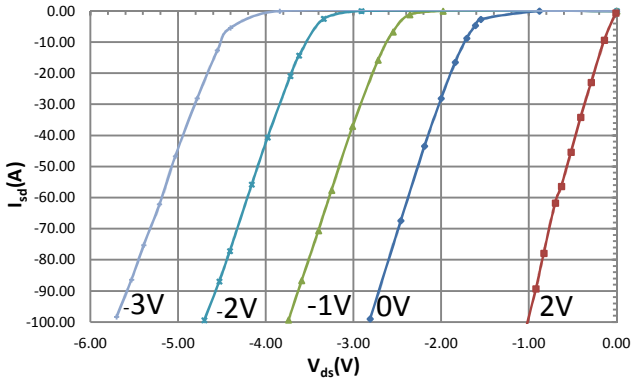



Figure 2.3 Measured reverse output I-V characteristics at room temperature 25ºC for EPC2001

The measured forward output characteristic curves ($V_{gs}$=2/3/4/5V) under operating temperatures 25°C and 125°C are shown in Fig 2.4. As seen, the slope of the I-V curve decreases with increasing temperature, indicating the decreasing channel conductivity. This is due to the lower channel carrier mobility under higher operating temperature. This device characteristic is potentially beneficial to device paralleling. Fig 2.5 shows the measured on-resistance at maximum gate-source voltage ($V_{gs}$=5V) as a function of junction temperature. The measured on-resistance of GaN HEMT increases from 6.01 mΩ to 10.01 mΩ, as device junction temperature rises from 25 ºC to 125 ºC.

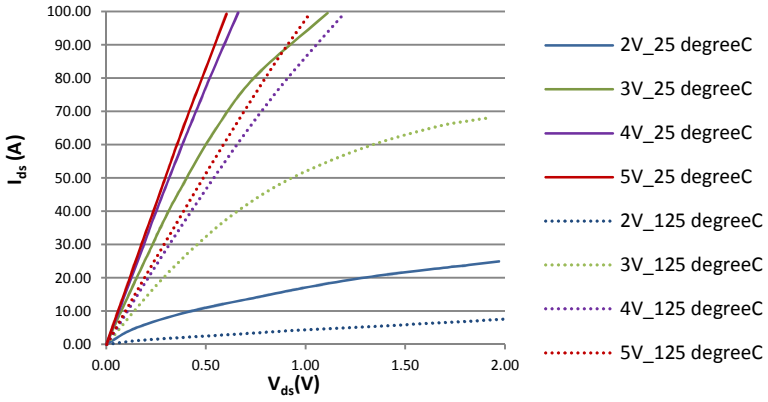



Figure 2.4 Measurement of forward output I-V characteristics at 25°C (solid) and 125 °C (dashed)

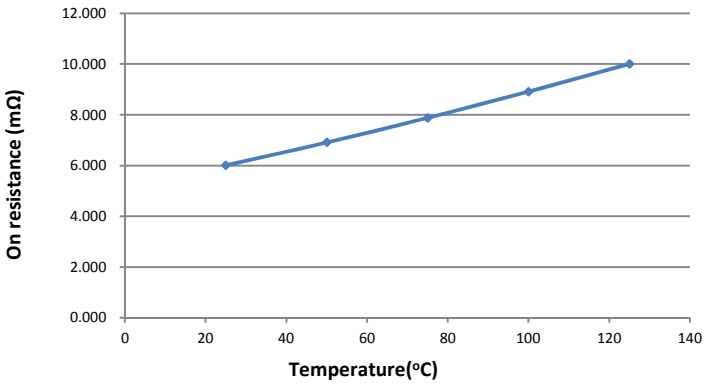



Figure 2.5 Measured on resistance of GaN HEMT at 5V gate-source voltage as a function of junction temperature

The measured reverse output characteristics curves ($V_{gs}$=-3/-2/-1/0/2V) under operating temperatures 25°C and 125°C show a similar behavior in Fig 2.6.

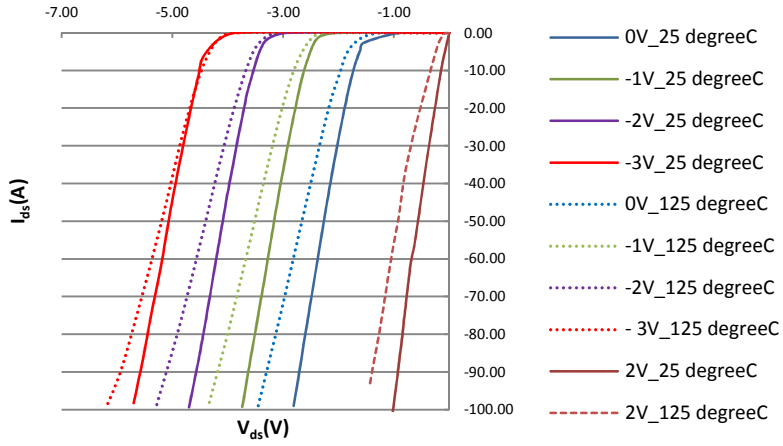



Figure 2.6 Measurement of reverse output I-V characteristics at 25°C (solid) and 125 °C (dashed)

The measured transfer characteristic of GaN HEMT at room temperature is shown in Fig 2.7, which describes drain current $I_{ds}$ as a function of gate-source voltage $V_{gs}$ at a constant drain-source voltage $V_{ds}$.

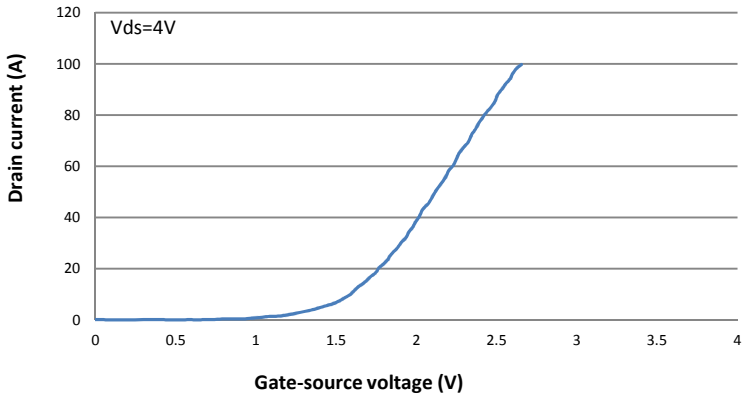



Figure 2.7 Measurement of transfer characteristics at room temperature 25°C

A plot of measured device parasitic capacitances is shown in Fig 2.8. These measurements justify the choice of having a constant gate-source capacitance $C_{gs}$, since from Fig 2.8 one can see that $C_{gs} = C_{iss} - C_{rss}$ is approximately constant.

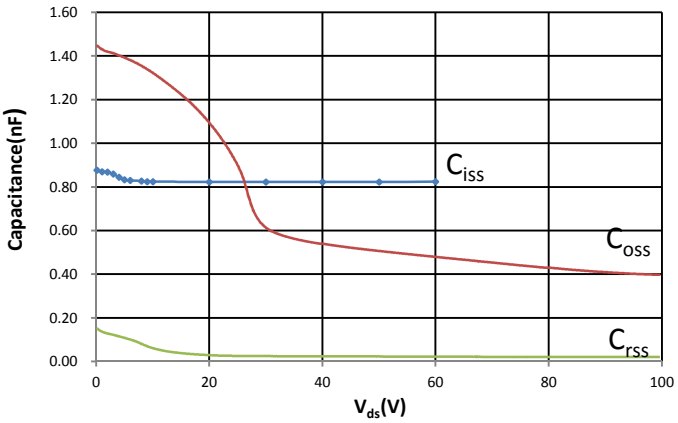



Figure 2.8 Measured capacitances versus drain-to-source voltage for EPC 2001

### 2.2.2 PARAMETER EXTRACTION

The parameter extraction process for GaN HEMT is developed using only measured static I-V and C-V characteristics. The parameter extraction procedure using static characterizations is described as follows:

1) Forward conduction device constant $K_{p1}$ and threshold voltage $V_{th1}$

A curve of the square root of $I_{ds}$ versus gate-source voltage $V_{gs}$ shown in Fig 2.9 is plotted to extract forward conduction device constant $K_{p1}$ and threshold voltage $V_{th1}$. The constant $(K_{p1}/2)^{0.5}$ is extracted from the slope of an operating point on the curve, when the GaN HMET operates in saturation region of forward conduction. The threshold voltage $V_{th1}$ is extracted from the point of intersection of the tangent line to the curve with the x-axis.

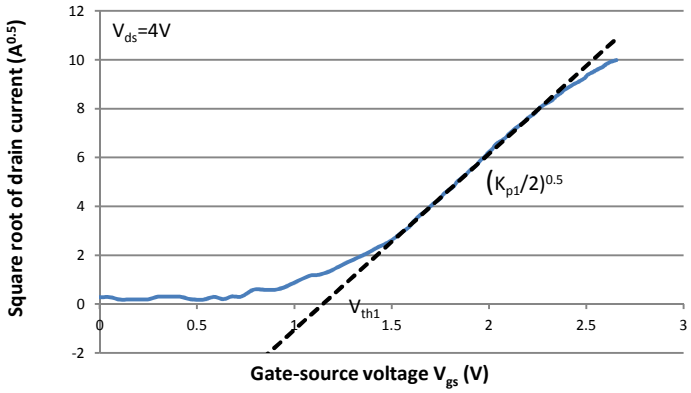



Figure 2.9 The plot of the square root of $I_{ds}$ vs. gate-source voltage

2) Forward conduction channel length modulation coefficient $\lambda_1$

The channel-length modulation coefficient $\lambda_1$ is extracted from the slope of forward output I-V characteristics in the saturation region.

3) Reverse conduction device constant $K_{p2}$ and threshold voltage $V_{th2}$

A curve of the square root of $I_{sd}$ versus gate-drain voltage $V_{gd}$ shown in Fig 2.10 is plotted to extract reverse conduction device constant $K_{p2}$ and threshold voltage $V_{th2}$. The constant $(K_{p2}/2)^{0.5}$ is extracted from the slope of an operating point on the curve, when the GaN HEMT operates in saturation region of reverse conduction. The threshold voltage $V_{th2}$ is extracted from the point of intersection of the tangent line to the curve.

4) Gate-source capacitance $C_{gs}$

The gate-source capacitance $C_{gs}$ is approximately constant. The parameter $C_{gs}$ is extracted from $C_{iss}$ and $C_{rss}$ measurements.

5) Zero-bias gate-drain capacitance $C_{gd0}$, built-in potential $PB_1$, and junction grading coefficient $m_1$:

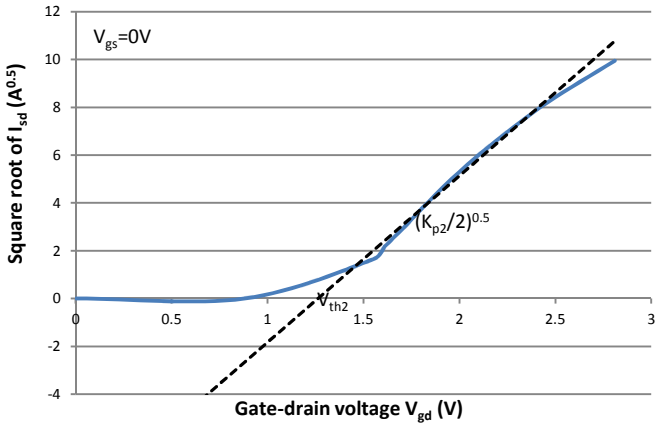



Figure 2.10 The plot of the square root of $I_{sd}$ vs. gate-drain voltage

The zero-bias gate-drain capacitance $C_{gd0}$ is extracted from $C_{rss}$ measurement at low gate-drain bias. As shown in Fig 2.11, the junction grading coefficient $m_1$ is extracted from the slope of gate-drain capacitance curve at high drain bias. The built-in potential $PB_1$ is extracted from a linear interpolation of the curve. The accuracy could be improved by using a higher order interpolation at the cost of increased model complexity.

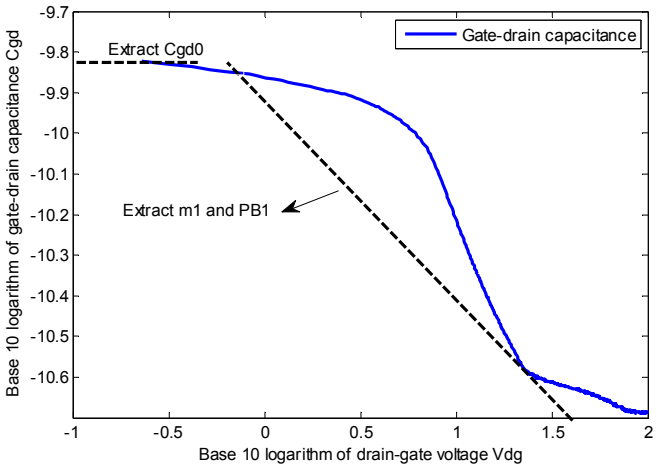



Figure 2.11 The log-log plot of $C_{gd}$ vs. drain-gate voltage

6) Zero-bias drain-source capacitance $C_{ds0}$, built-in potential $PB_2$, and junction grading coefficient $m_2$:

The zero-bias gate-drain capacitance $C_{ds0}$ is extracted from $C_{oss}$ and $C_{rss}$ measurements at low drain-source bias. As shown in Fig 2.12, the junction grading coefficient $m_2$ is extracted from the slope of drain-source capacitance curve at high drain bias. The built-in potential $PB_2$ is extracted from a linear interpolation to the curve.

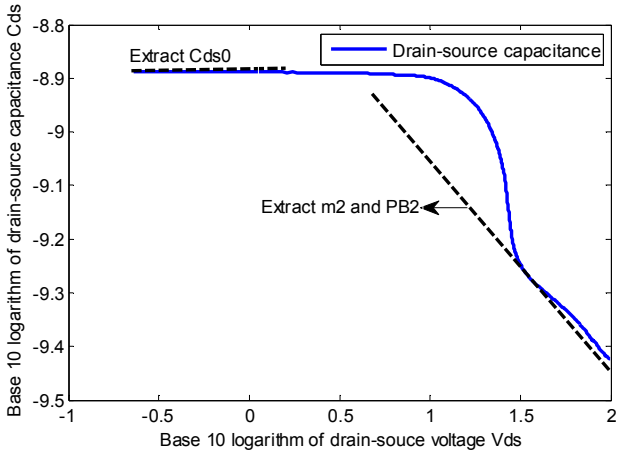



Figure 2.12 The log-log plot of $C_{ds}$ vs. drain-source voltage

7) Drain parasitic resistance $R_d$, and source parasitic resistance $R_s$

The total forward conduction on-resistances at varied gate-source voltages are extracted from output characteristics shown in Fig 2.13. In the linear I-V region, the parasitic resistances $R_d$ and $R_s$ are connected in series with the internal channel resistance.

With on-resistances extracted from Fig 2.13, a curve of total on-resistance as a function of $1/(V_{gs}-V_{th1})$ is given in Fig 2.14 to estimate the sum of parasitic resistances $R_d$ and $R_s$. The sum of $R_d$ and $R_s$ is extracted from the point of intersection of tangent line to the curve with the y-axis [38].

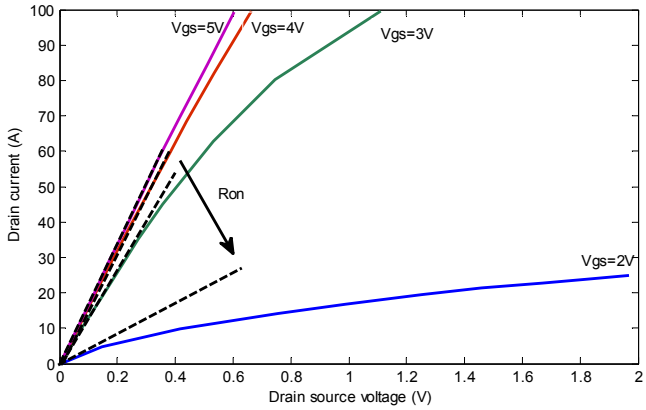



Figure 2.13 Forward conduction output characteristics and on-resistance extraction

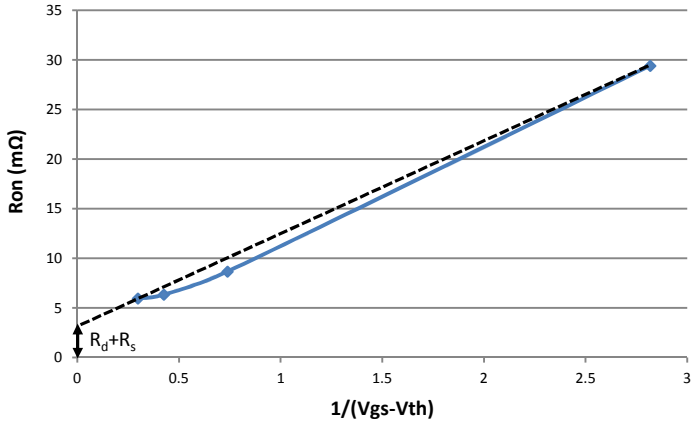



Figure 2.14 The plot of on-resistance $R_{on}$ vs. $1/(V_{gs}-V_{th1})$

Considering the lateral device structure of GaN HEMT, drain parasitic resistance $R_d$ is much larger than source parasitic resistance $R_s$. Therefore, source parasitic resistance $R_s$ is assumed to be zero in this model.

8) Temperature coefficients $T_{c1\_1}$, $T_{c1\_2}$, $T_{c2\_1}$, and $T_{c2\_2}$

Only parameters $K_{p1}$ and $K_{p2}$ have temperature dependence. To extract the temperature coefficients, the same extraction procedure for parameter $K_{p1}$ and $K_{p2}$ are performed at several higher temperatures. Only the temperature-dependent parameters are extracted at each temperature, while the temperature-independent parameters are fixed at

their room temperature values. Values for parameters $K_{p1}$ and $K_{p2}$ are obtained at several temperature points. Using temperature dependence equation (2-10), the temperature coefficients are extracted using the parameter values as a function of temperature.

## 2.3 Model Validation

The parameter extraction method of GaN HEMT model is described in this section. Table 2.2 lists the extracted model parameter values for EPC 2001 (100V/25A) GaN HEMT. In this section, the developed GaN HEMT model is validated under static and switching conditions.

Table 2.2 Extracted model parameter values for EPC 2001

| Parameter | Value | Source |
|---|---|---|
| $K_{p1}$ | 103.664A/V$^2$ | DC transfer characteristics |
| $K_{p2}$ | 102.259A/V$^2$ | DC transfer characteristics |
| $V_{th1}$ | 1.265 V | DC transfer characteristics |
| $V_{th2}$ | 1.285 V | DC transfer characteristics |
| $\lambda_1$ | 0.241 A/V | DC output characteristics |
| $C_{gs}$ | 0.804 nF | C-V characteristics |
| $C_{gd0}$ | 0.151 nF | C-V characteristics |
| $PB_1$ | 1.216 V | C-V characteristics |
| $m_1$ | 0.451 | C-V characteristics |
| $C_{ds0}$ | 1.299 nF | C-V characteristics |
| $PB_2$ | 1.805 V | C-V characteristics |
| $m_2$ | 0.302 | C-V characteristics |
| $R_d$ | 2.400 mΩ | DC output characteristics |
| $T_{c1\text{-}1}$ | 0.013 | Temperature |
| $T_{c2\text{-}1}$ | 1.906╳10$^{-5}$ | Temperature |
| $T_{c1\text{-}2}$ | 0.002 | Temperature |
| $T_{c2\text{-}2}$ | 6.241╳10$^{-5}$ | Temperature |

### 2.3.1 Validation of Static Characteristics

Fig 2.15 shows the comparison of simulated (dash lines) I-V characteristics of GaN HEMT in forward conduction mode based on the extracted parameters with

experimental (solid lines) static characteristics. The simulation I-V curves are in good agreement with experimental data under different gate bias conditions, however, some discrepancies can be observed in the saturation region. In order to capture the device on-state behavior, accurate modeling of the output characteristics in the linear region is crucial. Fig 2.16 shows the comparison of simulated (dash lines) I-V characteristics of GaN HEMT in the forward linear region based on the extracted parameters with experimental (solid lines) static characteristics. Good agreement between measured and simulated results is shown. Fig 2.17 shows the comparison between simulation (dash lines) I-V curves and experimental I-V characteristics (solid lines) in reverse conduction mode. The simulation results have very good matching with experimental results.

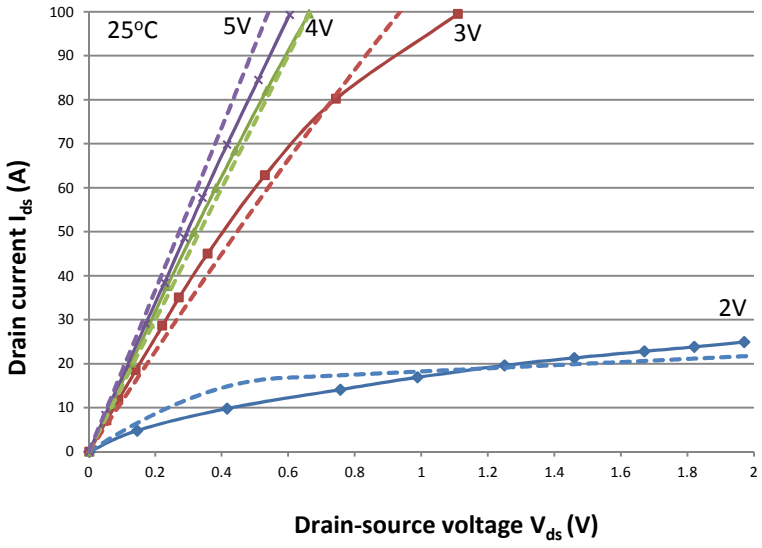



Figure 2.15 Forward I-V characteristics comparison between simulation (dashed) and measurement (solid) at room temperature 25°C

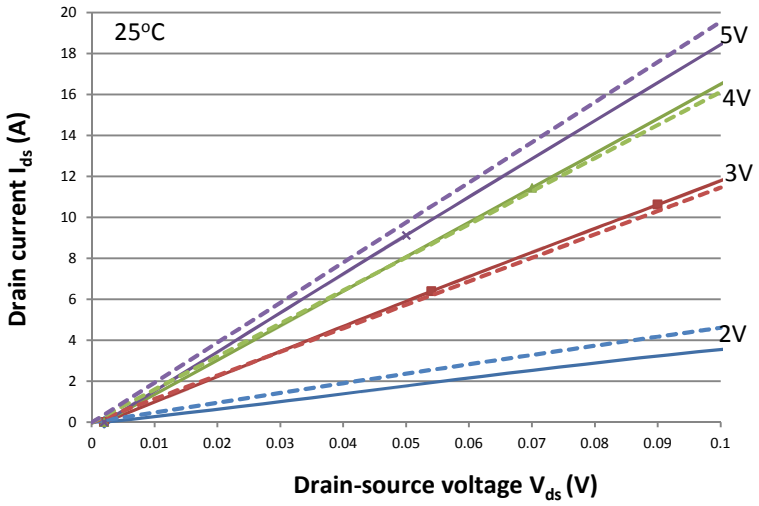



Figure 2.16 Forward I-V characteristics comparison between simulation (dashed) and measurement (solid) in linear region (zoom-in of prior figure) at room temperature 25°C

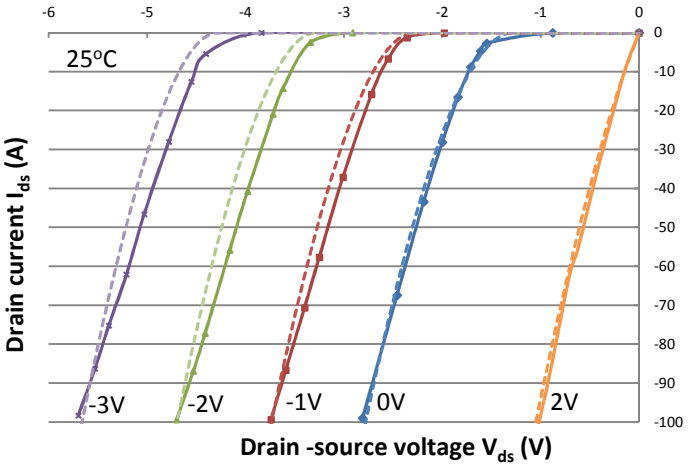



Figure 2.17 Reverse I-V characteristics comparison between simulation (dashed) and measurement (solid) at room temperature 25°C

The measured (solid lines) and simulated (dash lines) I-V characteristics in forward conduction mode at 125°C are shown in Fig 2.18. Fig 2.19 shows the measured (solid lines) and simulated (dash lines) I-V characteristics in reverse conduction mode. Excellent agreement is observed between simulation and measurement in I-V characteristics at 125°C. The comparison of on-resistance at maximum gate voltage

($V_{gs}$=5V) between simulations and experiments is shown in Fig 2.20. The simulated on-resistance is in agreement with the measured result over the temperature ranging from 25°C to 125°C.

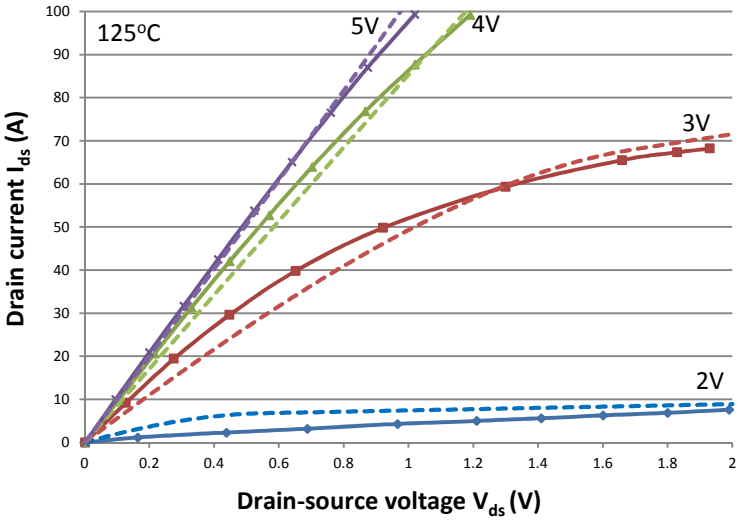



Figure 2.18 Forward I-V characteristics comparison between simulation (dashed) and measurement (solid) at 125°C

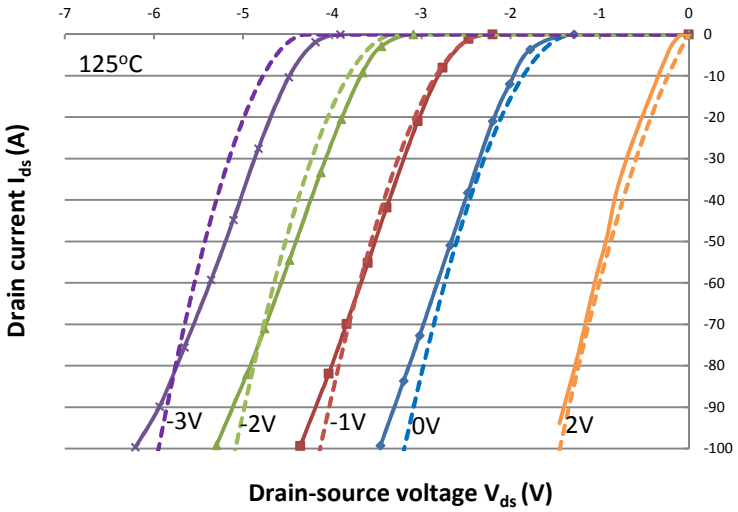



Figure 2.19 Reverse I-V characteristics comparison between simulation (dashed) and measurement (solid) at 125°C

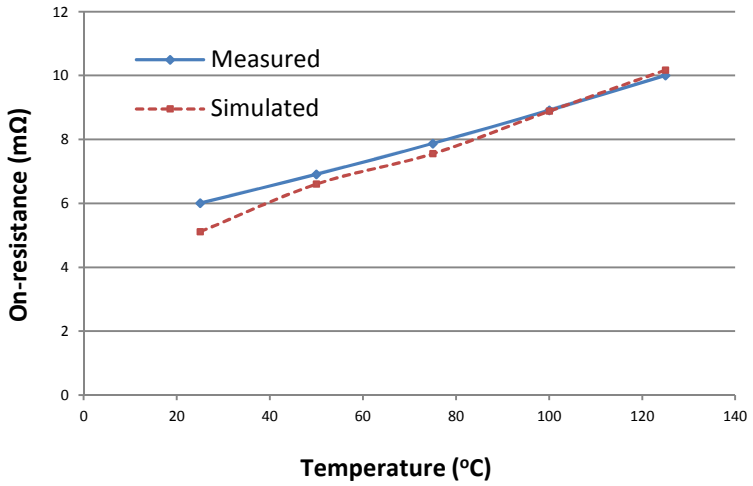



Figure 2.20 On-resistance comparison between simulation (dashed) and measurement (solid) at 5V gate-source voltage

Fig 2.21 shows the plot of measured and simulated capacitances of GaN HEMT, showing a discrepancy in the $C_{oss}$ voltage dependence at low drain voltages. This is probably due to two-dimensional effects at low voltage bias.

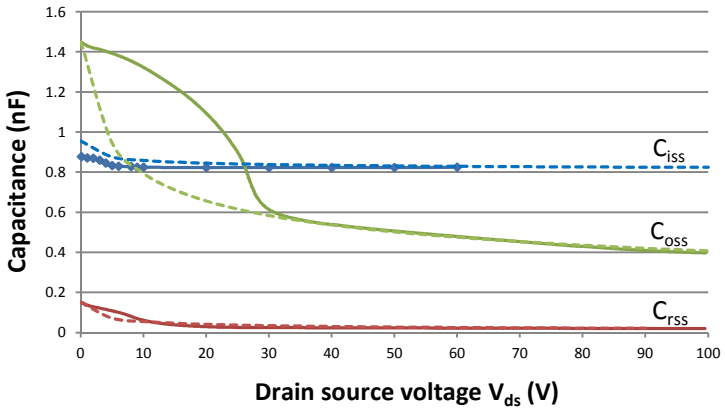



Figure 2.21 Comparison of C-V characteristics between simulation (dashed) and measurement (solid)

### 2.3.2 Validation of Switching Characteristics

A PCB double pulse tester circuit has been built to verify the accuracy of the proposed GaN HEMT device model under switching conditions. Fig 2.22 and Fig 2.23

show the double pulse test circuit schematic and PCB prototype. The double pulse test circuit has a phase leg structure with a GaN HEMT EPC 2001 pair. The PCB layout is carefully designed to minimize parasitic elements. The current waveforms are measured by a coaxial shunt resistor (0.1Ω) with high bandwidth and low parasitics from T&M Research Products, Inc. The gate driver is driver IC LM5113 from Texas Instruments, which is designed to drive both high side and low side enhancement mode GaN HEMTs in a half bridge configuration. The gate driver LM5113 has separate turn-on and turn-off driving pins, so that different gate resistances can be used for turn-on and for turn-off. Switching characterization is done under resistive load conditions and inductive load conditions at room temperature.

The 3-D inductance extraction software program FastHenry is used to estimate parasitic inductances in the DPT circuit PCB layout [39]. The circuit components in the double pulse tester, including load inductor, load resistor and current shunt are modeled on the basis of frequency domain measurements performed using the Agilent 4395A network analyzer. These parasitic are included in circuit simulations, in order to predict voltage and current transient slopes, ringing and spikes [40].

1) Resistive switching validation

For the resistive switching experiments the resistive load is 12 Ω. Switching speeds and energy losses are dependent on gate resistance values. Different gate driver turn-on and turn-off resistance values are tested. The top GaN HEMT device is off in this testing. The comparison between simulation and experiment is performed at room temperature. Comparisons between experimental and simulated waveforms are shown in

Fig 2.24 for turn-on transient and in Fig 2.25 for turn-off transient. The gate driver turn-on resistance is 7.5 Ω, and turn-off resistance is 3 Ω. As seen from the figures, the simulation results are in good agreement with the experimental results.

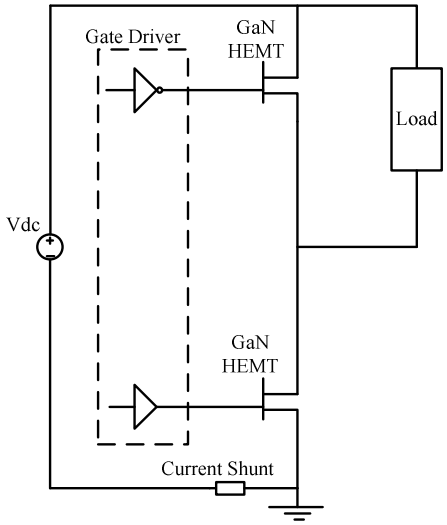



Figure 2.22 Double pulse test schematic

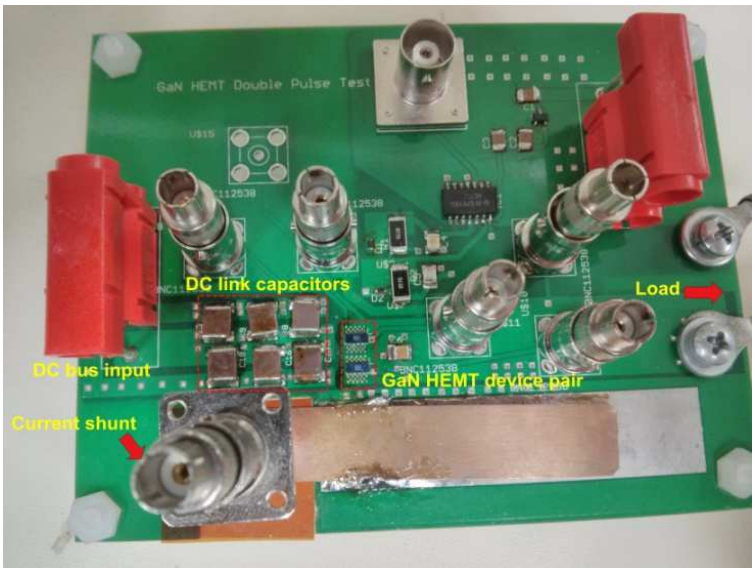



Figure 2.23 Picture of double pulse tester PCB board

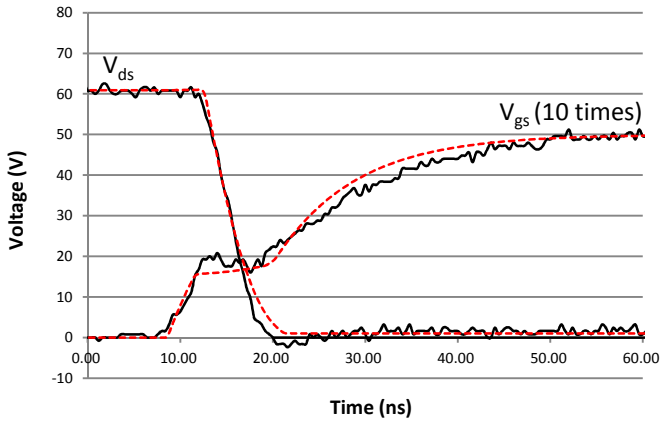



Figure 2.24 Simulated (dashed) and experimental (solid) turn-on voltage waveforms of resistive switching

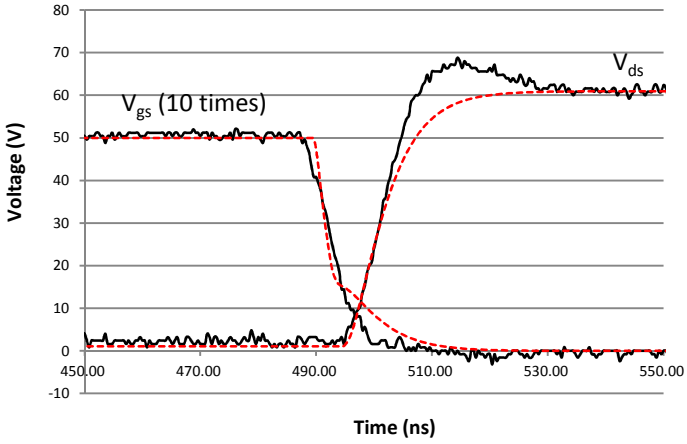



Figure 2.25 Simulated (dashed) and experimental (solid) turn-off voltage waveforms of resistive switching

Table 2.3 shows EPC 2001 turn-on and turn-off resistive switching performance with different gate resistance values. The fastest switching speeds obtained for the double pulse tester are $dV/dt_{(on)}$=16.2 V/ns, and $dV/dt_{(off)}$=26.6 V/ns. Fig 2.26 shows the turn-on speed dependence on turn-on resistance, while Fig 2.27 shows the turn-off speed dependence on turn-off resistance. As the gate resistance increases, switching speed reduces as expected. As turn-on gate resistance varies from 7.5 Ω to 15 Ω, the corresponding turn-on dV/dt drops from 9.34 V/ns to 5.42 V/ns. As turn-off gate

resistance increases from 3 Ω to 10 Ω, the corresponding turn-off dV/dt is reduced from 5.17 V/ns to 2.84 V/ns.

Table 2.3 Resistive switching results

| Turn on gate resistance $R_{on}$ (Ω) | Turn off gate resistance $R_{off}$ (Ω) | Turn on dv/dt (V/ns) | Drain-source voltage falling time (ns) | Turn off dv/dt (V/ns) | Drain-source voltage rising time (ns) |
|---|---|---|---|---|---|
| 15 | 10 | 5.42 | 8.9 | 2.84 | 16.9 |
| 15 | 7.5 | 5.42 | 8.7 | 3.29 | 14.6 |
| 15 | 3 | 5.51 | 8.7 | 4.98 | 9.6 |
| 10 | 3 | 7.42 | 6.5 | 5.00 | 9.6 |
| 7.5 | 3 | 9.34 | 5.2 | 5.17 | 9.3 |
| 0 | 0 | 16.2 | 3.0 | 26.6 | 1.78 |

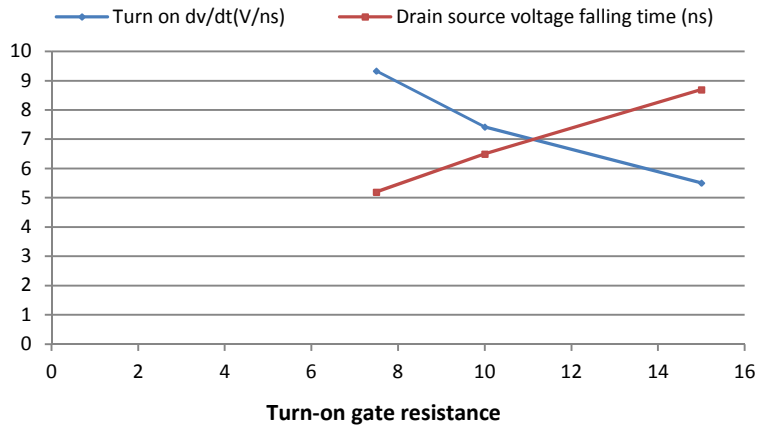



Figure 2.26 Turn-on dV/dt and drain source voltage falling time dependence on turn-on gate resistance

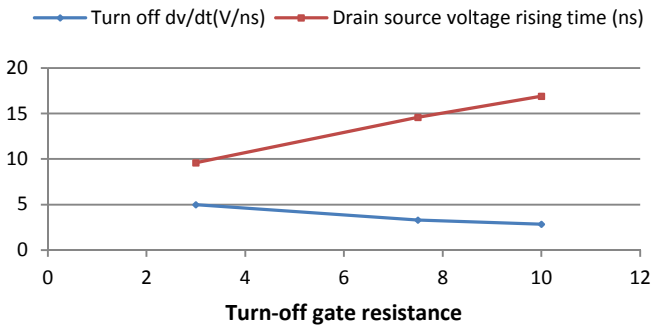



Figure 2.27 Turn-off dV/dt and drain source voltage rising time dependence on turn-off gate resistance

2) Inductive switching validation

For the inductive switching test a 250μH ferrite EE core inductor is used as an inductive load in the phase-leg tester topology. The inductor is modeled by adding to the main inductance an equivalent series resistance, an equivalent parallel capacitance, as well as an equivalent parallel resistance. By curve fitting the measured inductor impedance measured with the network analyzer, these parameters of the load inductor can be extracted. Fig 2.28 and Fig 2.29 show the inductive switching transient for the turn-on and turn-off of the low-side device under 48V dc voltage and 10A load current, with turn-on resistance 15 Ω and turn-off resistance 7.5 Ω. A good matching between simulation and measurement voltage waveforms is observed.

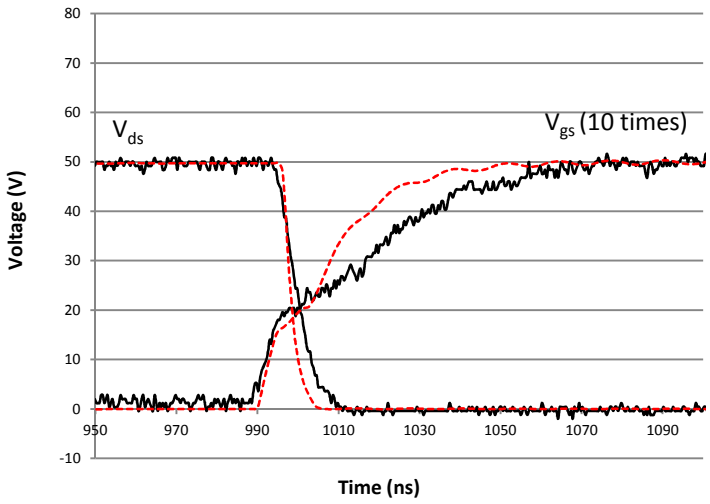



Figure 2.28 Simulated (dashed) and experimental (solid) turn-on voltage waveforms of inductive switching

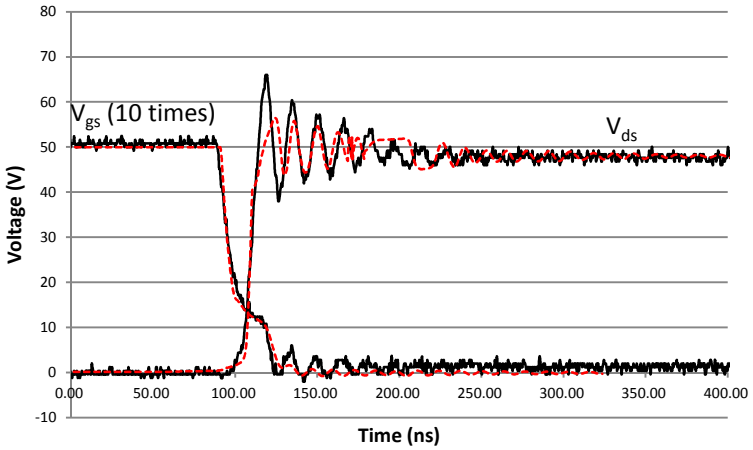



Figure 2.29 Simulated (dashed) and experimental (solid) turn-off voltage waveforms of inductive switching

Fig 2.30 and Fig 2.31 show the drain current waveforms during turn-on and turn-off transient under 10A inductive switching condition. Both turn-on and turn-off drain current transient comparisons show a good agreement.

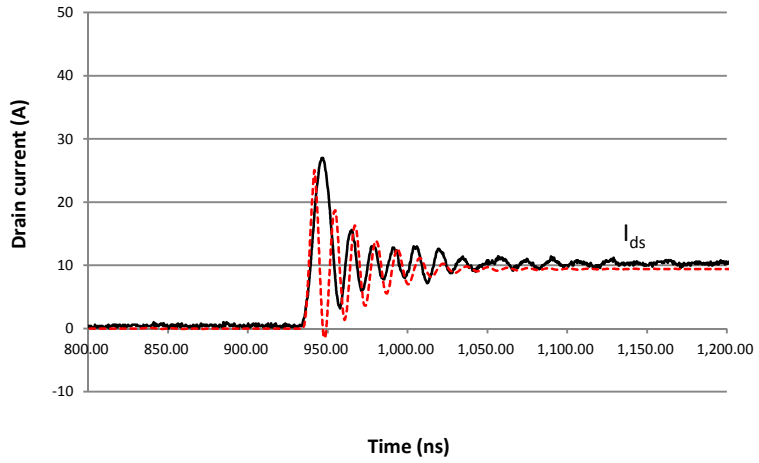



Figure 2.30 Simulated (dashed) and experimental (solid) turn-on current waveforms of inductive switching

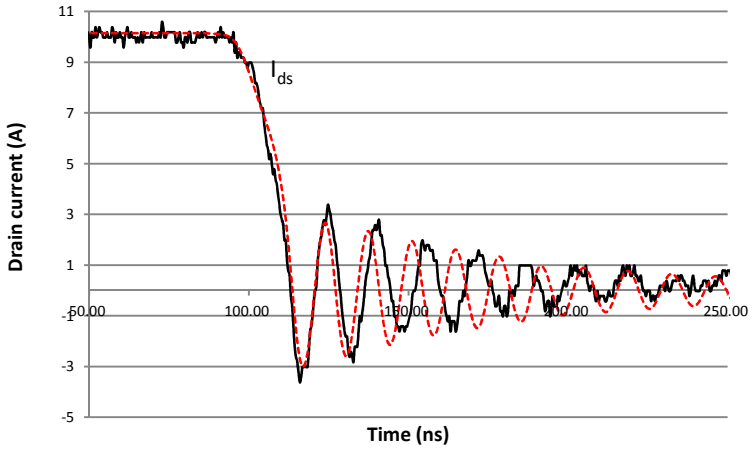


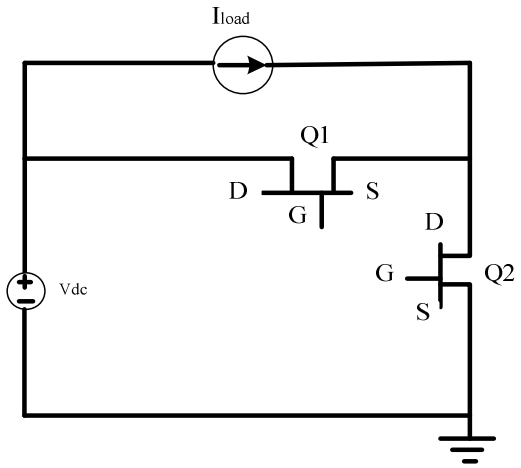

Figure 2.31 Simulated (dashed) and experimental (solid) turn-off current waveforms of inductive switching

3) Validation of 3rd quadrant operation

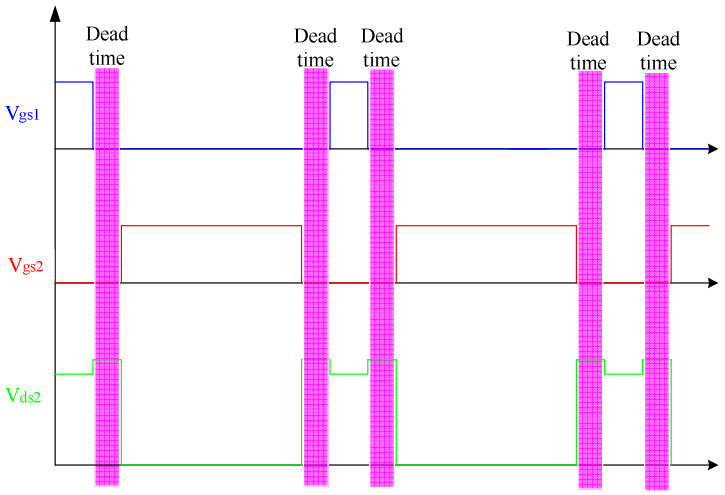
Considering the double pulse test circuit under inductive load shown in Fig 2.32a, the top side GaN HEMT Q1 operates as a free-wheeling diode. One main difference between a GaN HEMT and a silicon MOSFET is that the GaN HEMT does not have a built-in body diode. When the GaN HEMT is used as a freewheeling diode, it actually operates in the third quadrant. With zero gate-source voltage bias, the GaN HEMT has a

voltage drop of almost 1.7V for 10A current as shown in Fig 2.3. Therefore, it is desirable to reduce this conduction loss by turning on the top HEMT similarly to synchronous rectifier operation for a MOSFET circuit [41]. A short 100ns dead time between the two gate drive signals is introduced to avoid cross-conduction, as shown in Fig 2.32b.

Fig 2.33 shows the drain-source voltage of the Q2 switch at turn-on. From the figure it can be seen that the drain-source voltage increases by about 1.7V during the 100ns dead time. This is due to the increased voltage drop across switch Q1 during the dead time. Fig 2.34 shows a zoom-in of the voltage during the dead time interval. Note that the simulation captures this effect and shows excellent agreement with the experiment.




(a)




(b)

Figure 2.32 (a) Double pulse test schematic (b) Gate drive signals showing the dead time introduced to prevent cross-conduction

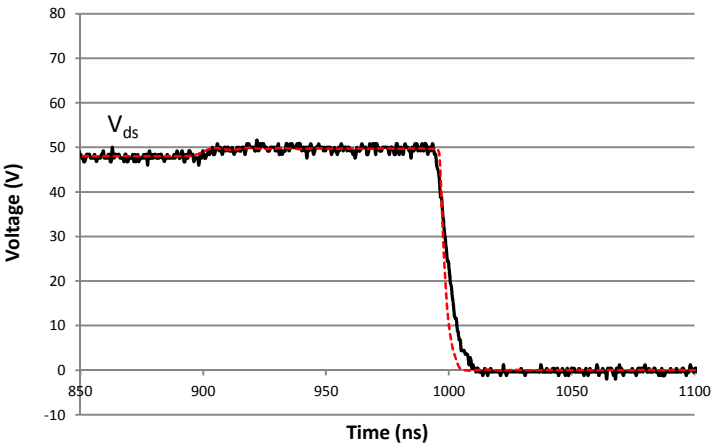



Figure 2.33 Comparison of simulated (dashed) and experimental (solid) drain-source voltage waveforms of Q2 at turn-on transition

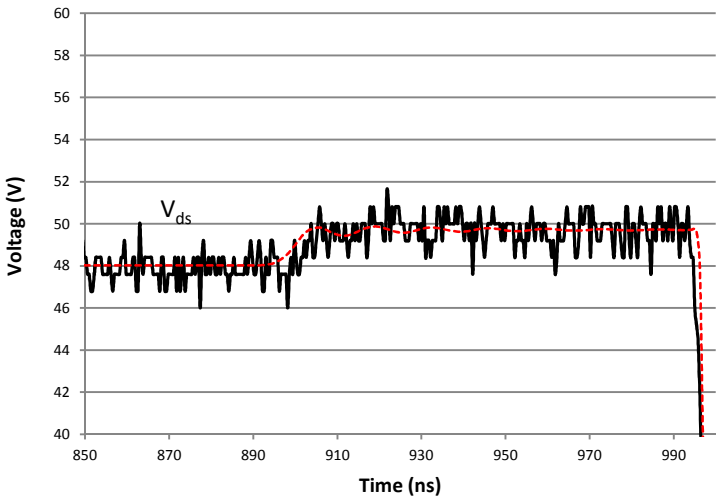



Figure 2.34 Comparison of simulated (dashed) and experimental (solid) drain-source voltage waveforms of Q2 at turn-on transition (zoom-in of prior figure)

## 2.4 SUMMARY

In this chapter, a simple and accurate circuit-simulator compact model for a normally-off GaN HEMT device is developed. The model parameters can be easily extracted from static I-V characteristics and C-V characteristics. This model captures reverse channel conduction, which is a very important feature for circuit designers. To the authors' knowledge this is the first GaN HEMT model that describes the complete static I-V characteristics for power electronics applications. A parameter extraction method is provided to allow easy extraction of model parameters using static I-V characteristics and C-V characteristics. The device model is validated under static conditions over a wide temperature range of 25ºC to 125ºC. A double pulse test-bench is built to test the switching behavior of GaN HEMT. In order to simulate the parasitic ringing during very fast switching transient, gate-to-source driving loop and drain-to-source main switching loop parasitic elements of the PCB layout are extracted using a 3-

D impedance extraction program. The extracted parameters are used with the GaN HEMT device models for resistive and inductive hard switching simulations in Pspice. The simulation results are compared with experimental results. The comparison shows good matching between simulated and experimental results under both resistive and inductive switching. The dynamic performance of the GaN HEMT in its reverse conduction region is also verified.

# CHAPTER 3

# CHARACTERIZATION AND MODELING OF SIC MOSFET BODY DIODE

SiC power MOSFET is a very good candidate for high-switching-frequency and low-loss power conversion applications [42][43][44][45]. The lower on-resistance makes SiC power MOSFETs an ideal choice in high power applications, offering similar conduction loss as Si IGBTs while operating at a much higher switching frequency. The switching loss of a SiC power MOSFET is much lower than that of a Si IGBT or Si GTO for the same voltage and current ratings, due to its lower device capacitance. In inductive hard switching, SiC MOSFET body diode might be used if no external anti-parallel diode is connected. For example, in a synchronous buck converter the inductor current flows through the lower MOSFET's body diode during the dead time periods [46]. In order to utilize the body diode of SiC MOSFET, a complete characterization (static and dynamic) of SiC MOSFET body diode is required. In addition, a circuit-oriented device model is needed to evaluate the performance of SiC MOSFET body diode in power converter design.

The body diode in a SiC power MOSFET is a p-i-n diode, as shown in Fig.3.1. The low-doped drift region is sandwiched between drain and source, creating a vertical body diode [47]. This p-i-n diode can be utilized to conduct current through the SiC power MOSFET in third quadrant operation. It is desirable to utilize MOSFET body

diodes to avoid additional cost of external anti-parallel diodes. However, a significant issue of body diode utilization is its reverse recovery. The reverse recovery is due to a large amount of injected carriers stored in the drift region during conduction. During the switch turn-off transition, some carriers are swept away from the drift region, resulting in reverse recovery current [48][49][50]. The reverse recovery current leads to additional switching loss in the complementary power switch.

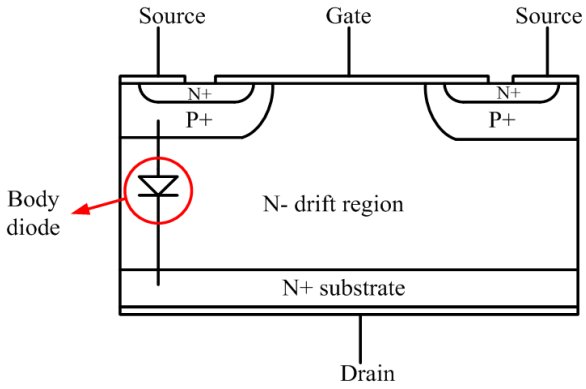



Figure 3.1 Cross-sectional structure schematic of power SiC DMOSFET

In this chapter, a complete performance characterization of SiC MOSFET body diode is carried out. The study is made for a 1200V/36A SiC MOSFET from Cree Inc. Static characterization is done using a curve tracer. For dynamic switching characterization, a double pulse tester (DPT) printed circuit board (PCB) with an inductive load is built. The reverse recovery of SiC MOSFET body diode is shown at different junction temperatures, current commutation slopes, and forward conduction currents. In addition, a Fourier-based-solution physics-based model for SiC MOSFET body diode is proposed. The parameter extraction procedure for SiC MOSFET body diode model is presented. Finally, the model is validated by comparing simulated results with experimental results under inductive switching condition.

## 3.1 STATIC CHARACTERISTICS

In this section, static characterization of SiC MOSFET body diode is described. Static characteristics (I-V) are measured with Tektronix 371A curve tracer. The device under test (DUT) is a SiC MOSFET C2M0080120D from CREE Inc. rated at 1200V/36A.

The static characterization of SiC MOSFET body diode is carried out at different gate-source voltages. Fig 3.2 shows the measured static characteristics (I-V) of SiC MOSFET body diode at room temperature, when gate-source voltage $V_{gs}$=0,5,10,15,20V.

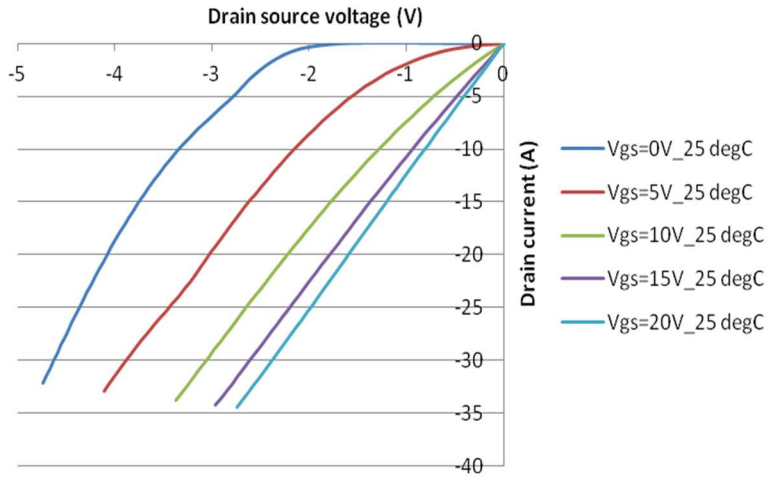



Figure 3.2 Static characteristics of SiC MOSFET body diode with positive gate-source voltages

As shown in Fig 3.2, when the gate-source voltage increases, more current flows through the MOSFET channel. As a result, the voltage between source and drain is reduced. When gate-source voltage reaches a value $V_{gs}$=20V, MOSFET channel is fully turned on, and MOSFET conducts in the third quadrant in a manner similar to forward conduction in the first quadrant.

Fig 3.3 shows the measured static characteristics (I-V) of SiC MOSFET body diode at room temperature, when gate-source voltage $V_{gs}$=0, -1, -2, -3, -4, -5V. As seen in Fig 3.3, as the gate-source voltage decreases, the voltage drop between source and drain increases.

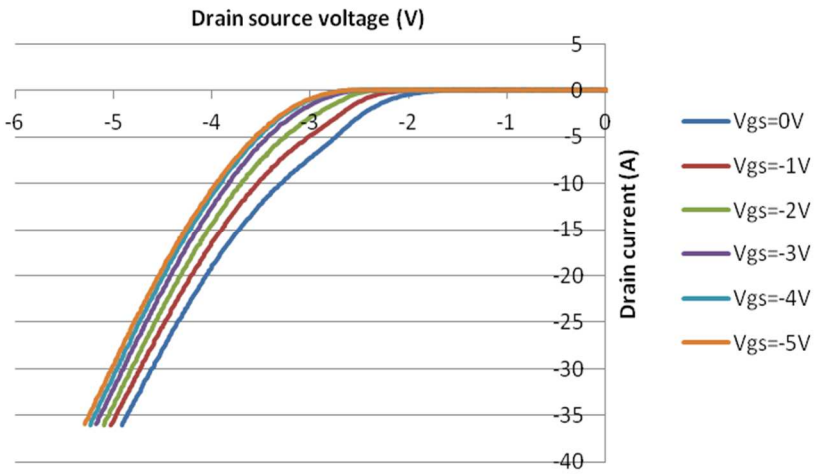



Figure 3.3 Static characteristics of SiC MOSFET body diode with negative gate-source voltages

Fig 3.4 shows the measured static characteristics (I-V) of SiC MOSFET body diode at junction temperatures 25ºC and 125ºC, when gate-source voltage $V_{gs}$=0, 5, 10, 15, 20V. Fig 3.5 shows the measured static characteristics (I-V) of SiC MOSFET body diode at junction temperatures 25ºC and 125ºC, when gate-source voltage $V_{gs}$=0, -2, -5V.

From Fig 3.4 and Fig 3.5, it can be seen that the MOSFET on-state resistance increases with junction temperature, due to lower carrier mobility at higher junction temperatures. In contrast, MOSFET body diode built-in voltage potential decreases with the increase of junction temperature, due to higher intrinsic carrier concentration at higher junction temperatures. The body diode series resistance also decreases with

junction temperature, because of higher minority carrier lifetime in drift layer at higher junction temperatures.

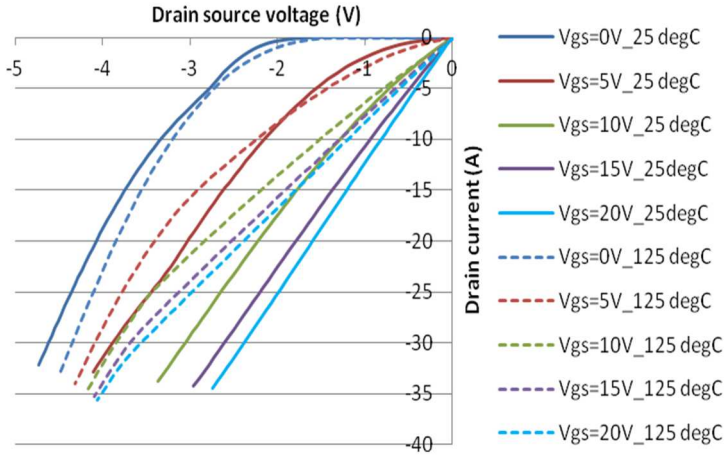



Figure 3.4 Static characteristics of SiC MOSFET body diode with positive gate-source voltages at 25ºC and 125ºC

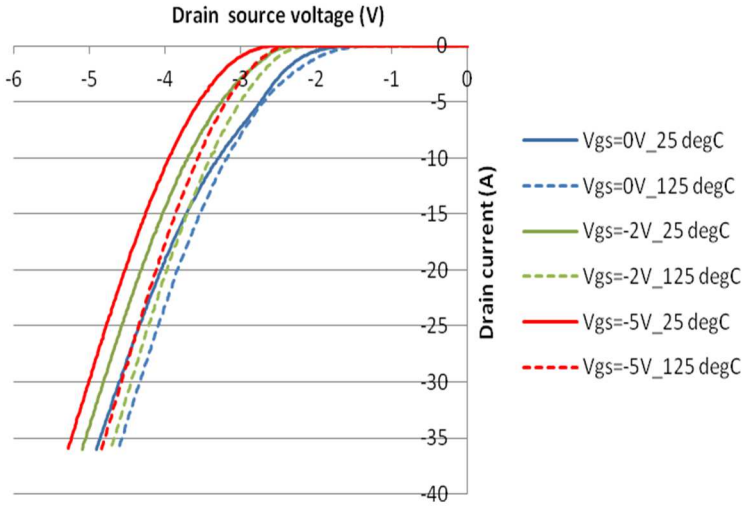



Figure 3.5 Static characteristics of SiC MOSFET body diode with negative gate-source voltages at 25ºC and 125ºC

Fig 3.6 shows the on-state resistance curve as a function of temperature, when $V_{gs}$=20V, and $I_{ds}$=18A. The on-state resistance is 79.6 mΩ at 25 ºC operating temperature, and the on-state resistance is 134.8 mΩ at 150 ºC operating temperature.

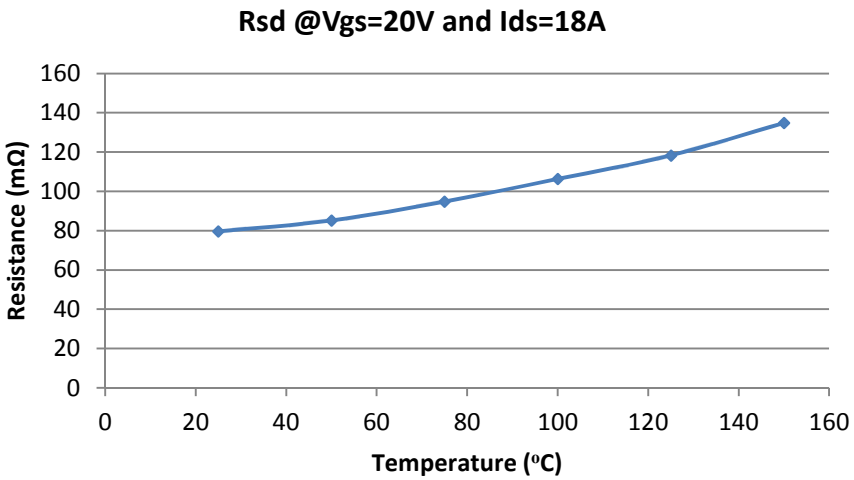



Figure 3.6 On-state resistance of SiC MOSFET as a function of temperature

Fig 3.7 shows body diode built-in potential curve as a function of temperature, when gate-source voltage $V_{gs}$=-5V. The body diode series resistance as a function of temperature is shown in Fig 3.8, when gate-source voltage $V_{gs}$=-5V.

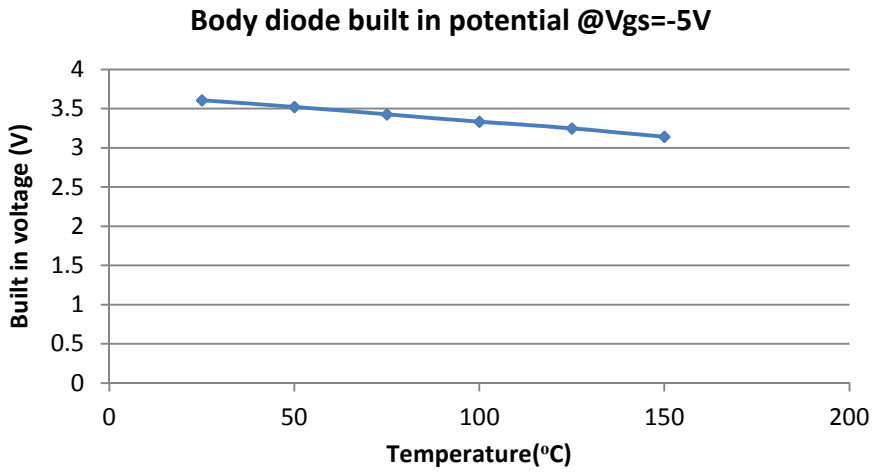



Figure 3.7 Body diode built-in potential of SiC MOSFET body diode as a function of temperature

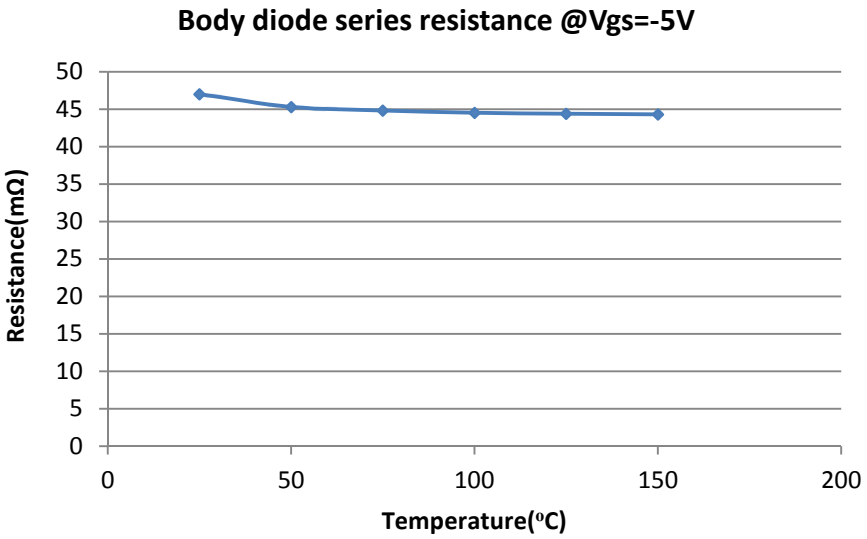



Figure 3.8 Body diode series resistance of SiC MOSFET body diode as a function of temperature

## 3.2 Double Pulse Tester

In order to study switching behavior of SiC MOSFET body diode, a printed circuit board (PCB) test-bench was built to conduct the inductive switching experiments on SiC power devices. The parasitic inductances from the PCB layout were minimized, when the PCB was designed. Fig.3.9 shows the schematic of double pulse tester for SiC MOSFET body diode switching characterization. Fig 3.10 shows the experimental setup of inductive switching.

The test-bench includes a test socket for high-side SiC MOSFET, a test socket for low-side SiC MOSFET, gate drive circuit, input capacitor bank, a load inductor, probe-tip-adapters, and a Pearson coil for drain current measurement. The MOSFET under test is a SiC MOSFET C2M0080120D from CREE Inc. rated at 1200V/36A. A gate driver IC IXDD609SI based on the totem-pole structure from IXYS Corporation is used as the SiC

MOSFET gate driver with 9A maximum source/sink drive current. A Pearson coil (model 2878) is used to measure the MOSFET body diode current. A 250 μH ferrite-core inductor is used as the load inductor for inductive switching experiments.

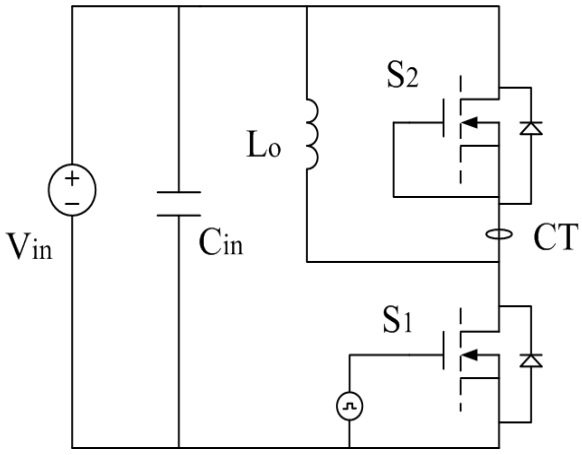



Figure 3.9 Schematic of double pulse tester

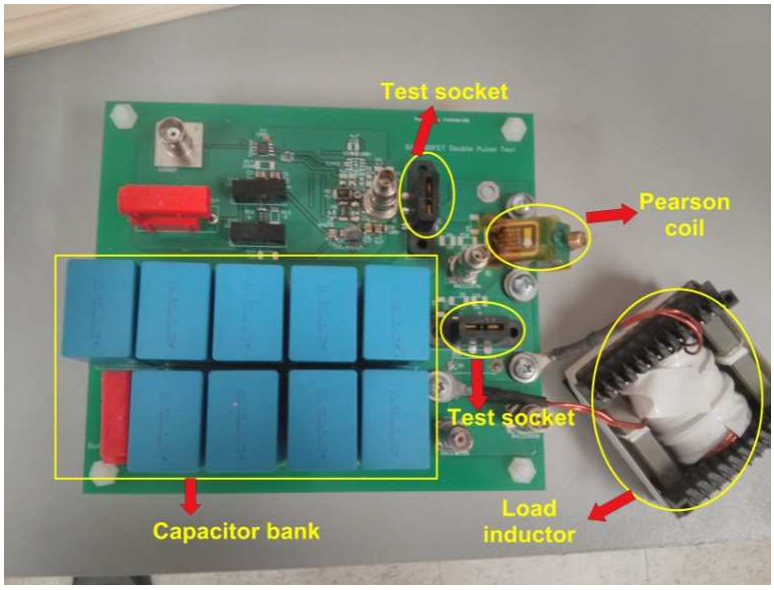



Figure 3.10 Picture of double pulse tester

## 3.3 SWITCHING CHARACTERISTICS

MOSFET body diode is based on the p-i-n diode structure, and a lightly n-doped layer is inserted between the n+ drain and the p body. During the turn-off transition of MOSFET body diode, the reverse recovery can be observed, because the minority carriers in the drift layer must be removed or recombined before the body diode can block a reverse voltage. Reverse recovery is the foremost characteristic of MOSFET body diode. In this section, the reverse current waveforms of SiC MOSFET body diode with varied gate resistances, forward conduction currents and temperatures are measured to evaluate the switching performance of SiC MOSFET body diode.

### 3.3.1 VARIED GATE RESISTANCES (CURRENT COMMUTATING SLOPES)

Fig 3.11 shows the experimental current waveforms with varied low-side MOSFET gate resistances at room temperature. The reverse recovery charge decreases with the increase of gate resistance, because more minority carriers recombine in longer reverse recovery time.

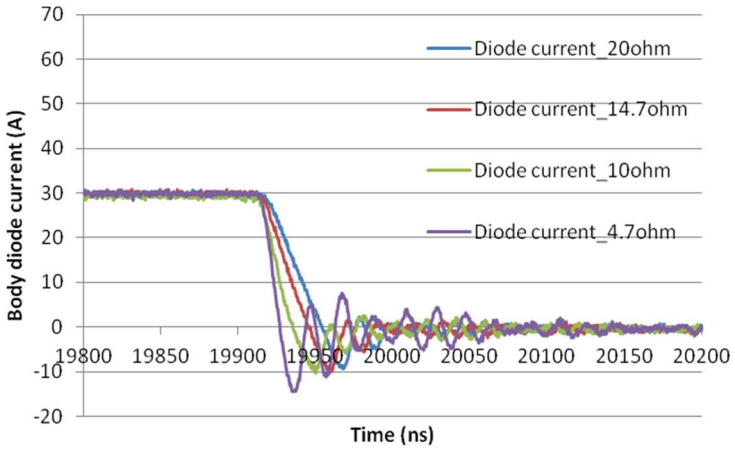



Figure 3.11 Body diode current waveforms at different low-side SiC MOSFET gate resistances (block voltage: 500V, forward conduction current: 30A)

Fig 3.12 gives the reverse peak currents and reverse recovery charges with varied low-side MOSFET gate resistances at room temperature. Both reverse peak current and reverse recovery charge decrease, as low-side SiC MOSFET gate resistance increases.

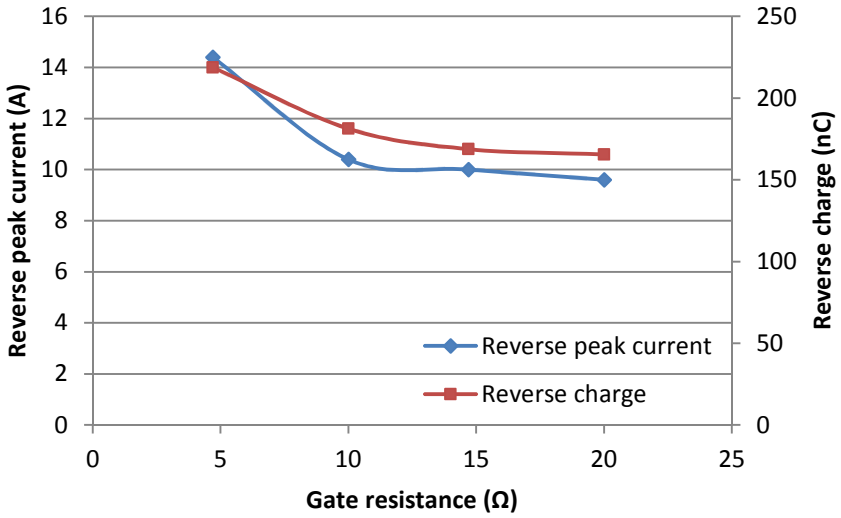



Figure 3.12 Body diode reverse peak currents and reverse recovery charges at different low-side MOSFET gate resistances (block voltage: 500V, forward conduction current: 30A)

Fig 3.13 shows the reverse recovery times and current commutating slopes (di/dt) with varied low-side MOSFET gate resistances at room temperature. As the low-side gate resistance increases, the current commutating slope (di/dt) decreases. By contrast, the reverse recovery time increases with the low-side MOSFET gate resistance.

Fig 3.14 shows switching losses from reverse recovery in body diode and switching losses from reverse current in the complementary switch with varied low-side MOSFET gate resistances at room temperature. As the low-side gate resistance increases, switching loss from reverse recovery in body diode and switching loss from reverse current in complementary switch reduce.

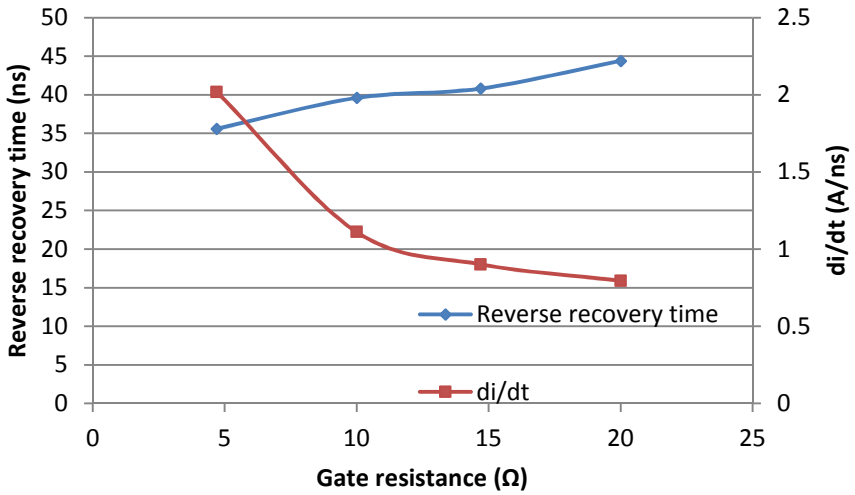



Figure 3.13 Body diode reverse recovery times and di/dt at different low-side MOSFET gate resistances (block voltage: 500V, forward conduction current: 30A)

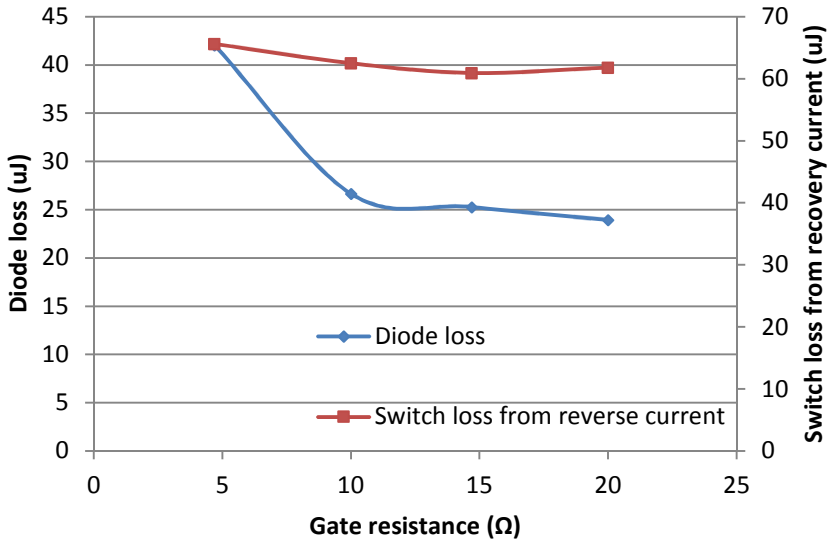



Figure 3.14 Body diode reverse recovery switching losses and switching losses from reverse current in complementary switch at different low-side MOSFET gate resistances (block voltage: 500V, forward conduction current: 30A)

### 3.3.2 VARIED FORWARD CONDUCTION CURRENTS

The body diode current waveforms in Fig 3.15 are measured with different forward conduction currents at gate resistance 20 Ω and room temperature. The reverse peak current and reverse charge increase with the forward conduction current. A higher forward conduction current requires more free charge in the drift region, which results in a larger reverse recovery.

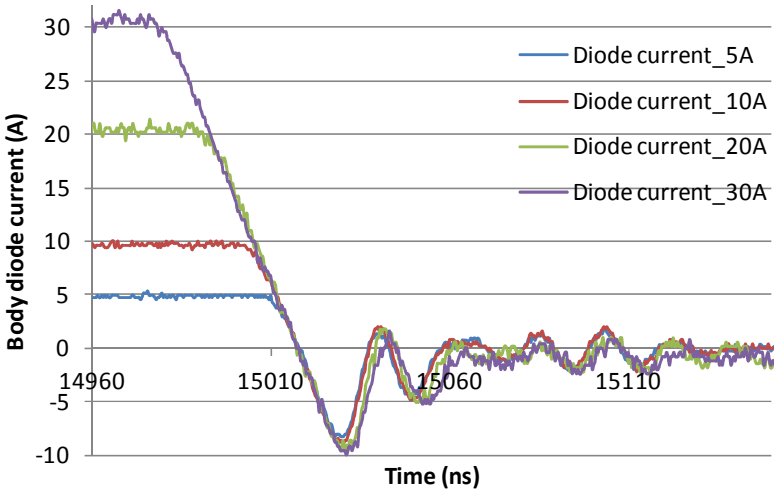



Figure 3.15 Body diode current waveforms at different forward conduction currents (block voltage: 500V, gate resistance: 20Ω)

Fig 3.16 shows the reverse peak current and reverse recovery charge with varied forward conduction currents at room temperature. Both reverse peak current and reverse recovery charge increase, as forward conduction current increases. However, the influence of forward current on reverse peak current is weak. The forward conduction current increases from 5A to 30A, but the reverse peak current only changes from 8A to 9.6A.

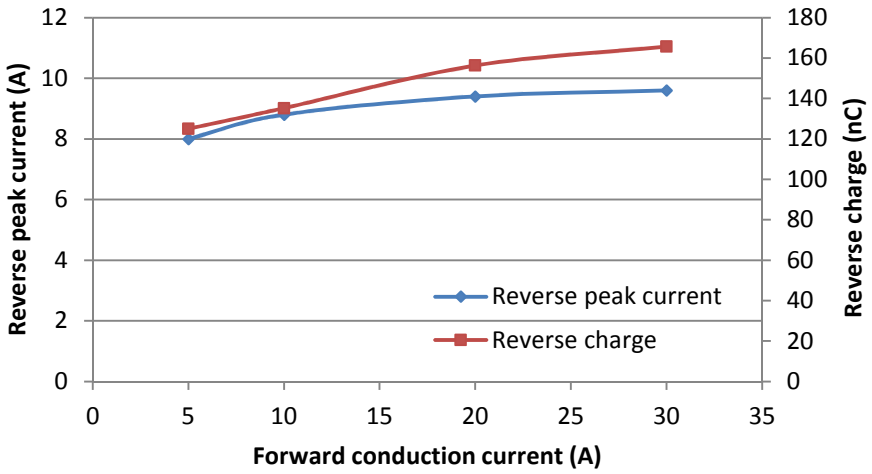



Figure 3.16 Body diode reverse peak currents and reverse charges at different forward conduction currents (block voltage: 500V, gate resistance: 20Ω)

Fig 3.17 shows the reverse recovery time as a function of forward conduction current at room temperature. As forward conduction current increases, the reverse recovery time of body diode increases.

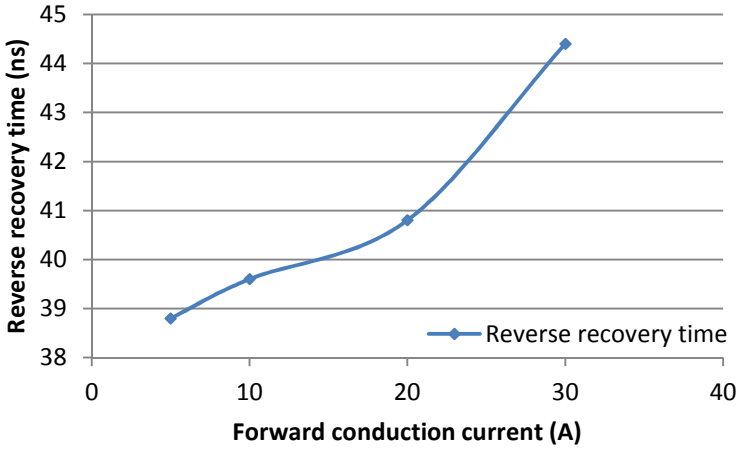



Figure 3.17 Body diode reverse recovery times at different forward conduction currents (block voltage: 500V, gate resistance: 20Ω)

Fig 3.18 shows switching loss from reverse recovery in body diode and switching loss from reverse recovery current in the complementary switch with varied forward

conduction currents at room temperature. As forward conduction current increases, both switching loss from reverse recovery in body diode and switching loss from reverse current in complementary switch increase.

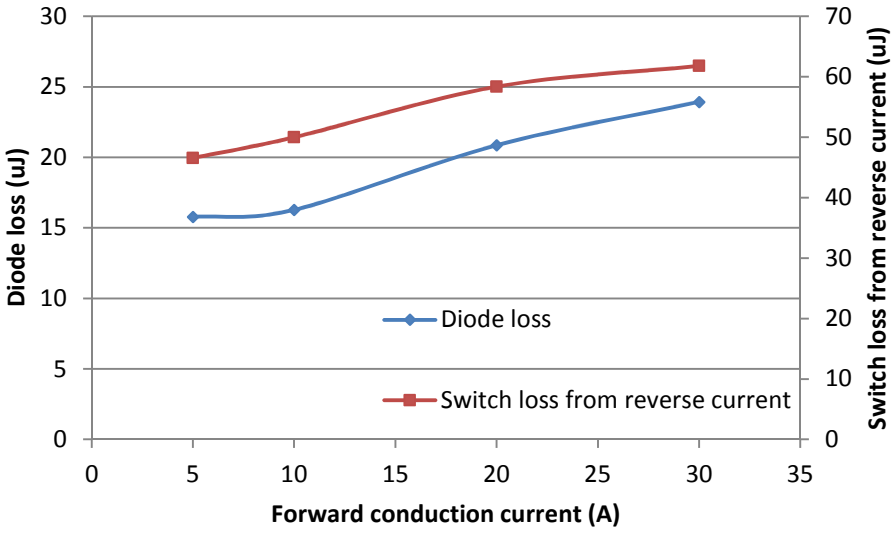



Figure 3.18 Body diode reverse recovery switching losses and switching losses from reverse current in complementary switch at different forward conduction currents (block voltage: 500V, gate resistance: 20Ω)

### 3.3.3 VARIED JUNCTION TEMPERATURES

The DUT is heated by attaching it to a heat spreader, whose temperature is controlled by a thermal controller Eurotherm 94 [51]. At each temperature operating point, the device is heated for a long enough time to ensure that MOSFET's junction temperature is equal to the case temperature. Fig 3.19 shows the experimental waveforms at varied junction temperatures. Both the reverse peak current and reverse recovery charge increase with junction temperature. Fig 3.20 shows the reverse peak current and reverse recovery charge as a function of junction temperature. Fig 3.21 shows the reverse recovery time as a function of junction temperature. Fig 3.22 gives switching loss from

reverse recovery in body diode and switching loss from reverse recovery current in the complementary switch with varied junction temperatures. As junction temperature increases, both diode switching loss from reverse recovery and switching loss from reverse current in complementary switch increase.

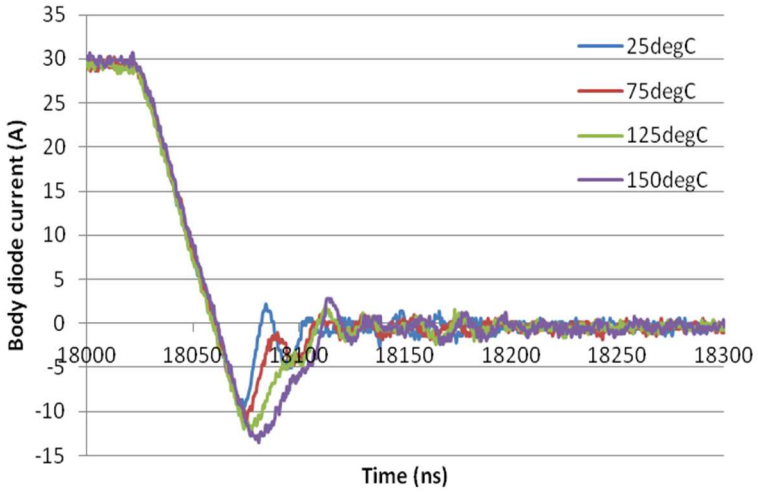



Figure 3.19 Body diode current waveforms at different temperatures (block voltage: 500V, gate resistance: 20Ω, forward conduction current: 30A)

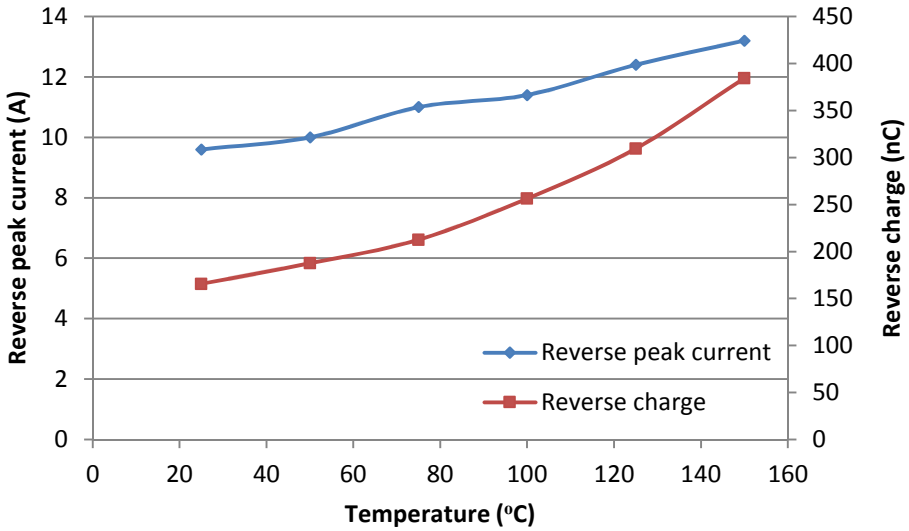



Figure 3.20 Body diode reverse peak current and reverse charge at different temperatures (block voltage: 500V, gate resistance: 20Ω, forward conduction current: 30A)

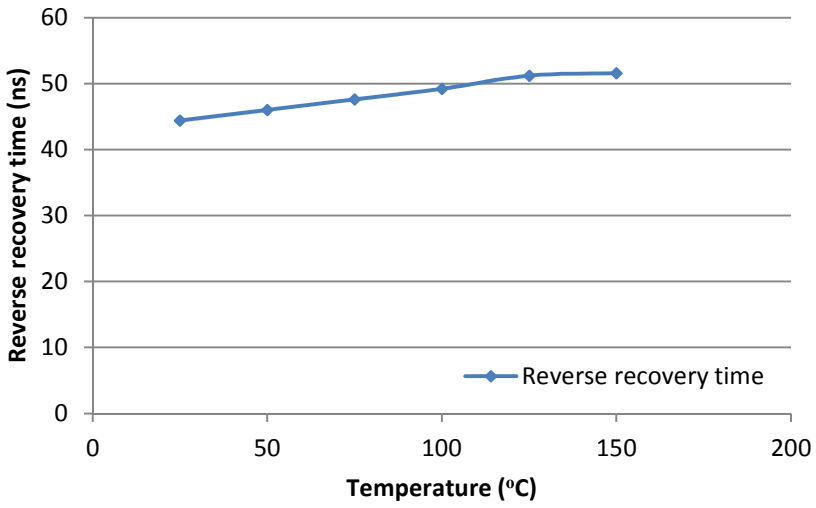



Figure 3.21 Body diode reverse recovery times at different temperatures (block voltage: 500V, gate resistance: 20Ω, forward conduction current: 30A)

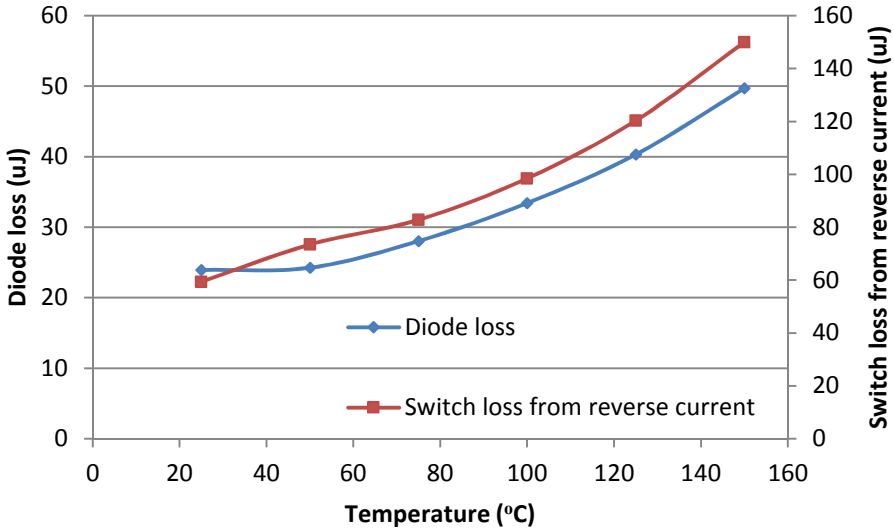



Figure 3.22 Body diode reverse recovery switching losses and switching losses from reverse current in complementary switch at different temperatures (block voltage: 500V, gate resistance: 20Ω, forward conduction current: 30A)

## 3.4 Body Diode Model Development

The body diode model uses a Fourier series solution of the ambipolar diffusion equation (ADE) in the drift layer to find the carrier distribution in that region [52][53][54][55][56]. This carrier distribution is used to find the conductive voltage drop in the drift region, accounting for conductivity modulation.

### 3.4.1 Solutions To ADE

Fig 3.23 shows the general arrangement of the carrier distribution in n- drift region, including an un-depleted carrier storage layer and two depletion layers [57]. The carrier storage layer is sandwiched between two depletion layers. When the body diode is on, the two depletion layers shrink, and the carrier storage layer occupies the whole drift region. When the body diode is off, the two depletion layers expand from the two ends of the drift region, and free carriers are swept from the carrier storage region. The depletion layers start to support a voltage and the body diode becomes reverse-biased.

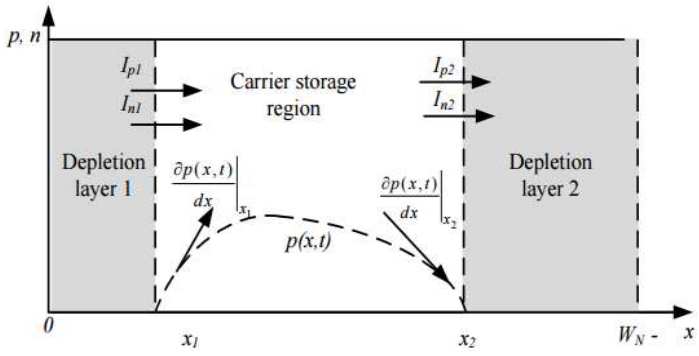



Figure 3.23 Carrier storage layer and depletions layers in n-drift region

Under high level injection, the ambipolar carrier diffusion equation (ADE) describes the carrier dynamics as follows:

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau} + \frac{\partial p(x,t)}{\partial t} \qquad \text{Equation 3-1}$$

where D is the ambipolar diffusion coefficient, τ is high-level carrier lifetime in the drift region, and p(x,t) is the carrier concentration as a function of space x and time t. The ambipolar diffusion equation is a 2nd order partial differential equation, which describes the minority carrier distribution profile in the drift region of bipolar devices, as a function of time and space.

A Fourier-series based solution to ADE is proposed, which converts the 2nd order partial differential equation into an infinite set of 1st order ordinary differential equations with coefficients $p_0 \ldots p_k$. The Fourier-series based solution is given by:

$$p(x,t) = p_0(t) + \sum_{k=1}^{\infty} p_k(t)\cos\left[\frac{k\pi(x-x_1)}{(x_2-x_1)}\right] \qquad \text{Equation 3-2}$$

where $x_1$ and $x_2$ are the boundaries of carrier storage region.

The Fourier series coefficients $p_k$ are given as follows:

$$p_0(t) = \frac{1}{x_2-x_1}\int_{x_1}^{x_2} p(x,t)dx \qquad \text{Equation 3-3}$$

$$p_k(t) = \frac{2}{x_2-x_1}\int_{x_1}^{x_2} p(x,t)\cos\left[\frac{k\pi(x-x_1)}{(x_2-x_1)}\right]dx \qquad \text{Equation 3-4}$$

By substituting equations (3-3) and (3-4) into equation (3-1), the Fourier-series coefficients $p_k$ are determined as the solution of an infinite set of 1st order linear differential equations. The boundary conditions at the boundaries of carrier stored region ($x_1$ and $x_2$) are required, which give the gradients of the carrier densities. The boundary conditions are given by:

$$\frac{\partial p}{\partial x}\Big|_{x_1} = \frac{1}{2qA}\left(\frac{I_n}{D_n} - \frac{I_p}{D_p}\right)\Big|_{x_1} \qquad \text{Equation 3-5}$$

$$\frac{\partial p}{\partial x}|_{x_2} = \frac{1}{2qA}\left(\frac{I_n}{D_n} - \frac{I_p}{D_p}\right)|_{x_2} \qquad \text{Equation 3-6}$$

where $D_n$ and $D_p$ are electron and hole diffusion coefficients, $I_n$ and $I_p$ are electron and hole currents, and A is the device chip active area.

The infinite set of 1st order linear differential equations is given by:

k=0:

$$\frac{D}{x_2 - x_1}\left[\frac{\partial p(x,t)}{\partial x}|_{x_2} - \frac{\partial p(x,t)}{\partial x}|_{x_1}\right] = \frac{dp_0(t)}{dt} + \frac{p_0(t)}{\tau} + \frac{1}{x_2 - x_1}\sum_{n=1}^{\infty}\left[\frac{dx_1}{dt} - (-1)^n \frac{dx_2}{dt}\right]p_n(t) \qquad \text{Equation 3-7}$$

k>0:

$$\frac{2D}{x_2 - x_1}\left[\frac{\partial p(x,t)}{\partial x}|_{x_2}(-1)^k - \frac{\partial p(x,t)}{\partial x}|_{x_1}\right] = \frac{dp_k(t)}{dt} + \left[\frac{1}{\tau} + \frac{Dk^2\pi^2}{(x_2 - x_1)^2}\right]p_k(t)$$
$$+ \frac{2}{x_2 - x_1}\left(\sum_{\substack{n=1 \\ n\neq k}}^{\infty}\left[\frac{dx_1}{dt} - (-1)^{n+k}\frac{dx_2}{dt}\right]p_n(t)\frac{n^2}{n^2 - k^2} + \frac{p_k}{4}\left(\frac{dx_1}{dt} - \frac{dx_2}{dt}\right)\right) \qquad \text{Equation 3-8}$$

The even harmonics and odd harmonics of the Fourier terms for the stored carrier charge can be represented using the electrical equivalent circuit shown in Fig 3.24.

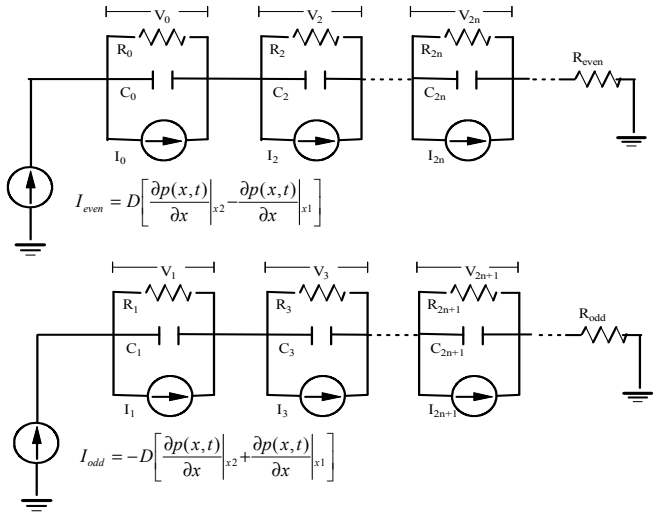



Figure 3.24 Equivalent circuit used to calculate the carrier density representing the coefficients of the Fourier series solution to ADE

At the boundaries $x_1$ and $x_2$, the carrier densities $p_{x1}$ and $p_{x2}$ are calculated using equation (3-9) and (3-10), respectively.

$$p_{x1} = \sum_{k=1}^{n} (-1)^k p_k \qquad \text{Equation 3-9}$$

$$p_{x2} = \sum_{k=1}^{n} p_k \qquad \text{Equation 3-10}$$

### 3.4.2 Diode Voltage Drop

The voltage drop across the body diode $V_{ak}$ is comprised of several components, including the voltages $V_{j1}$ and $V_{j2}$ across junctions $J_1$ and $J_2$, the voltages $V_{d1}$ and $V_{d2}$ across two depletion layers, and the voltage $V_{n-}$ across the n- drift region.

$$V_{ak} = V_{j1} + V_{d1} + V_{n-} + V_{d2} + V_{j2} \qquad \text{Equation 3-11}$$

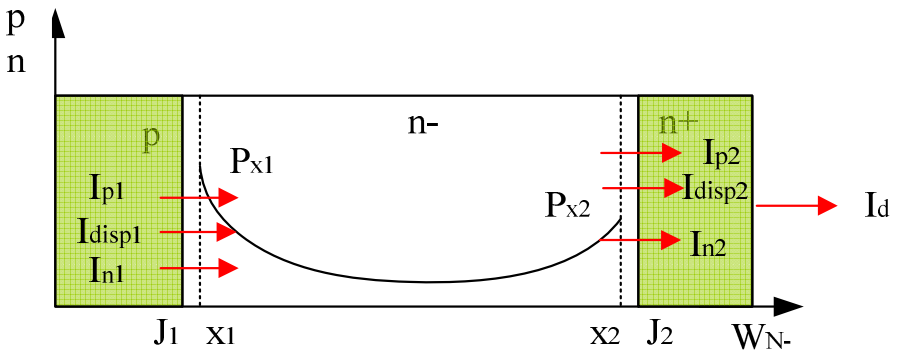



Figure 3.25 Schematic structure and carrier densities of drift region of a SiC MOSFET body diode during on-state

The voltage $V_{n-}$ across the undepleted low-doped drift region is calculated based on the current through this region. The current transport equations for electrons and holes are given by [58]:

$$J_n = q\mu_n nE + qD_n \frac{\partial n}{\partial x} \qquad \text{Equation 3-12}$$

$$J_p = q\mu_p pE - qD_p \frac{\partial p}{\partial x} \qquad \text{Equation 3-13}$$

Due to high level injection, charge neutrality requires that the carrier densities for electrons and holes be equal in the carrier storage region:

$$n = p + N_{N-} \qquad \text{Equation 3-14}$$

where $N_{N-}$ is the doping concentration of the drift region.

The total current density J is given by:

$$J = J_p + J_n = qE[p(\mu_n + \mu_p) + \mu_n N_{N-}] + qV_T(\mu_n - \mu_p)\frac{\partial p}{\partial x} \qquad \text{Equation 3-15}$$

where $V_T$ is equal to kT/q.

The electric field E, is given by:

$$E = \frac{J}{q[p(\mu_n + \mu_p) + \mu_n N_{N-}]} - \frac{V_T(\mu_n - \mu_p)}{p(\mu_n + \mu_p) + \mu_n N_{N-}}\frac{\partial p}{\partial x} \qquad \text{Equation 3-16}$$

The drift region voltage $V_{n-}$ is calculated by integrating the electrical field through the undepleted region with two boundaries $x_1$ and $x_2$.

$$V_{N-} = \int_{x_1}^{x_2} \frac{J}{q[p(\mu_n + \mu_p) + \mu_n N_{N-}]} dx - \int_{p_{x1}}^{p_{x2}} \frac{V_T(\mu_n - \mu_p)}{p(\mu_n + \mu_p) + \mu_n N_{N-}} \partial p \qquad \text{Equation 3-17}$$

In order to simplify the calculation of the drift region voltage $V_{n-}$, the discretized carrier distribution shown in Fig 3.26 is used, and the carrier storage region is divided into several segments of equal width. In the carrier profile, a straight line is used to connect two adjacent points. The tradeoff between accuracy and simulation speed is made by selecting the number of segments.

Assuming that the number of segments is M, the width of segment is given by:

$$\Delta x = \frac{x_2 - x_1}{M} \qquad \text{Equation 3-18}$$

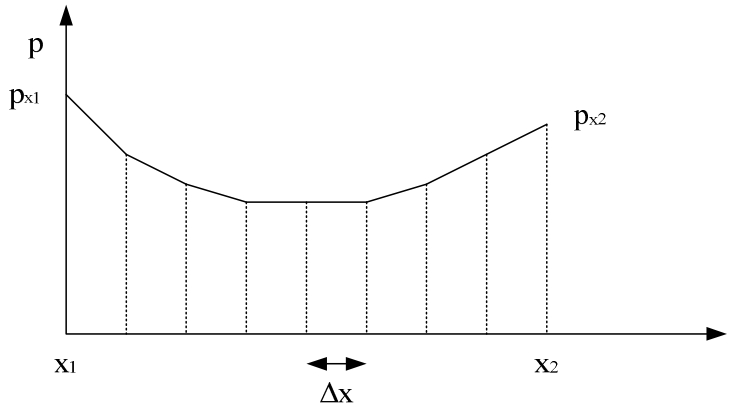



Figure 3.26 Discretized carrier profile for simulation of $V_{n-}$

The carrier density distribution between two adjacent points is approximated to be a straight line.

$$P_T = P_{T1} + (P_{T2} - P_{T1})\frac{x}{\Delta x} \qquad \text{Equation 3-19}$$

The voltage drop for each segment in carrier storage region is calculated by:

$$V_{seg} = \frac{J}{q(\mu_n + \mu_p)} \int_0^{\Delta x} \frac{dx}{P_T} = \frac{J}{q(\mu_n + \mu_p)} \frac{\Delta x}{P_{T2} - P_{T1}} \ln(\frac{P_{T2}}{P_{T1}}) \qquad \text{Equation 3-20}$$

The drift region voltage $V_{n-}$ in carrier storage region is calculated by:

$$V_{n-} = \frac{I_d}{qA(\mu_n + \mu_p)} \frac{x_2 - x_1}{M} \sum_{k=0}^{M} [\frac{1}{P_{T(k)} - P_{T(k-1)}} \ln(\frac{P_{T(k)}}{P_{T(k-1)}})] - V_T(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}) \ln(\frac{P_{x2}}{P_{x1}}) \qquad \text{Equation 3-21}$$

where $I_d$ is the body diode conduction current, A is the active area, and M is the number of segments in carrier storage region.

The junction voltage of $J_1$ is given by:

$$V_{j1} = V_T \ln(\frac{P_{x1} N_{N-}}{n_i^2}) \qquad \text{Equation 3-22}$$

where $n_i$ is the intrinsic carrier concentration in SiC, and $P_{x1}$ is the carrier density at the boundary $x_1$.

The junction voltage of $J_2$ is given by:

$$V_{j2} = V_T \ln(\frac{P_{x2}}{N_{N-}}) \qquad \text{Equation 3-23}$$

where $P_{x2}$ is the carrier density at the boundary $x_2$.

The depletion layer voltages $V_{d1}$ and $V_{d2}$ are derived using feedback from the carrier densities $P_{x1}$ and $P_{x2}$ at boundaries [59]:

$$V_{d1} = \begin{cases} 0 & if \quad P_{x1} > 0 \\ -K_F P_{x1} & otherwise \end{cases} \qquad \text{Equation 3-24}$$

$$V_{d2} = \begin{cases} 0 & if \quad P_{x2} > 0 \\ -K_F P_{x2} & otherwise \end{cases} \qquad \text{Equation 3-25}$$

where $K_F$ is the feedback constant.

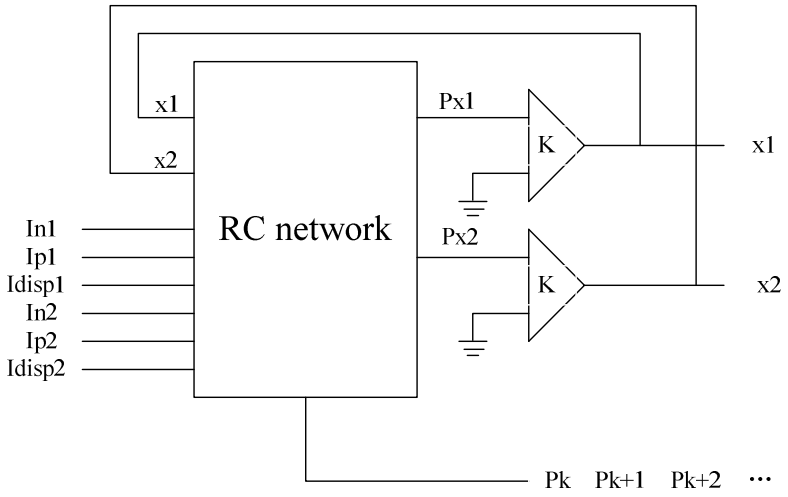



Figure 3.27 Feedback scheme for the calculation of $x_1$ and $x_2$

The widths of depletion layers, $W_{d1}$ and $W_{d2}$, are given by:

$$W_{d1} = \sqrt{\frac{2\varepsilon_{SiC} V_{d1}}{qN_{N-} + I_d / (Av_{sat})}} \qquad \text{Equation 3-26}$$

$$W_{d2} = \sqrt{\frac{2\varepsilon_{SiC} V_{d2}}{qN_{N-} + I_d / (Av_{sat})}} \qquad \text{Equation 3-27}$$

where $N_{N-}$ is the doping concentration in the drift region, $I_d$ is the total diode current, and $V_{sat}$ is the saturation drift velocity.

The boundaries $x_1$ and $x_2$ are calculated by:

$$x_1 = W_{d1} \qquad \text{Equation 3-28}$$

$$x_2 = W_{N-} - W_{d2} \qquad \text{Equation 3-29}$$

where $W_{N-}$ is the total length of low-doped n- drift region.

### 3.4.3 Current Components

The injection of minority carriers into the end regions should be taken into account. Fig 3.28 shows the p region with current components $I_{p1}$, $I_{n1}$, and $I_{disp1}$. The p region is high-doped, and minority electrons are injected into p region due to high level injection during the on-state. The minority electrons recombine with holes in p region. This carrier recombination results in electron current $I_{n1}$.

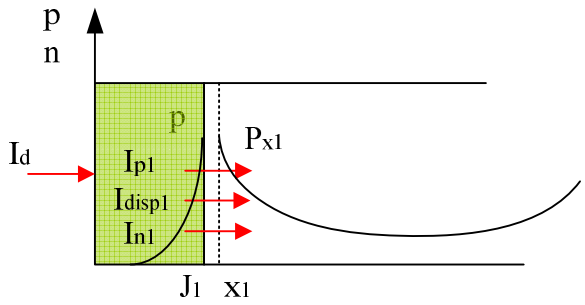



Figure 3.28 Carrier distribution and currents in p end region of the body diode during the on-state

The electron current $I_{n1}$ in the p end region is given by:

$$I_{n1} = qAh_p P_{x1}^2 \qquad \text{Equation 3-30}$$

where $h_p$ is the recombination parameter, and $P_{x1}$ is the carrier density at the boundary $x_1$. Note that under high level injection the hole and electron densities in the drift region are locally approximately equal, due to quasi-neutrality.

The displacement current $I_{disp1}$ in the p end region is calculated by:

$$I_{disp1} = \varepsilon A \frac{1}{W_{d1}} \frac{dV_{d1}}{dt} \qquad \text{Equation 3-31}$$

According to current continuity at junction $J_1$, the total diode current is given by:

$$I_d = I_{n1} + I_{p1} + I_{disp1} \qquad \text{Equation 3-32}$$

Fig 3.29 shows the n+ region with current components $I_{p2}$, $I_{n2}$, and $I_{disp2}$. The n+ region is high-doped, and minority holes are injected into n+ region due to high level injection during the on-state. Minority holes are recombined with electrons in the n+ region. This carrier recombination results in hole current $I_{p2}$.

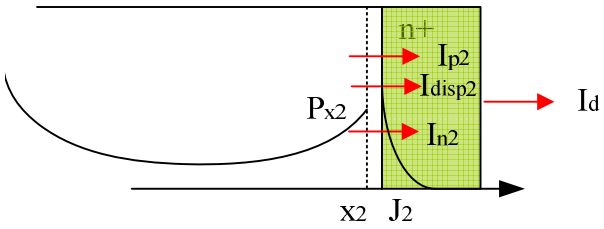



Figure 3.29 Carrier distribution and currents in n+ end region of the body diode during the on-state

The hole current $I_{p2}$ in the n+ end region is given by:

$$I_{p2} = qAh_n P_{x2}^2 \qquad \text{Equation 3-33}$$

where $h_n$ is the recombination parameter, and $P_{x2}$ is the carrier density at the boundary $x_2$.

The displacement current $I_{disp2}$ in the n+ end region is calculated by:

$$I_{disp2} = \varepsilon A \frac{1}{W_{d2}} \frac{dV_{d2}}{dt} \qquad \text{Equation 3-34}$$

According to current continuity at junction $J_2$, the total diode current is given by:

$$I_d = I_{n2} + I_{p2} + I_{disp2}$$ Equation 3-35

## 3.5 Parameter Extraction

The body diode model parameters are listed in Table 3.1. Only six parameters are needed for this body diode model, and they can be estimated from manufacturer's datasheets or from diode's turn-off waveforms.

Table 3.1 Body diode model parameter list

| Symbol | Description |
|---|---|
| A ($cm^2$) | Chip active area |
| τ (μs) | High-level minority carrier lifetime |
| $W_{N-}$ (μm) | Drift region width |
| $N_{N-}$ ($cm^{-3}$) | Doping concentration in drift region |
| $h_p$ ($cm^4/s$) | Recombination parameter in p region |
| $h_n$ ($cm^4/s$) | Recombination parameter in n+ region |

The parameter extraction procedure includes an initial parameter estimation from the manufacturer's datasheet, and a parameter refinement based on the measured switching waveforms [60].

### 3.5.1 Initial Parameter Estimation

1) Chip active area A: The chip active area can be obtained from datasheet or be roughly estimated from the maximum current density J (about $300A/cm^2$) and current rating $I_d$.

The chip active area A is calculated by:

$$A = \frac{I_d}{J} \qquad \text{Equation 3-36}$$

2) The high-level minority carrier lifetime τ can be initially estimated using the equation:

$$\tau = \frac{Q_{rr}}{I_F} \qquad \text{Equation 3-37}$$

where $Q_{rr}$ is the reverse recovery charge in device datasheet, and $I_F$ is the forward conduction current in the datasheet.

3) The ionization coefficients for electrons and holes, which are electric field dependent, are given by:

$$\alpha_{n,p} = a \exp(-b / E) \qquad \text{Equation 3-38}$$

where a and b are the constants, and E is the electric field.

Assuming avalanche breakdown in an abrupt junction, the equation for the breakdown voltage $V_{BD}$ as a function of the constants a and b, and n- drift region width $W_{N-}$, can be given by:

$$V_{BD} = \frac{bW_{N-}}{\ln(aW_{N-})} \qquad \text{Equation 3-39}$$

The drift region width $W_{N-}$ can be derived from equation (3-39), using $a=3.25\times 10^6$ $cm^{-1}$, and $b=1.75\times 10^7$ V/cm. The breakdown voltage $V_{BD}$ is the voltage rating in the manufacturer's datasheet plus some safety margin.

4) From the empirical effective impurity doping concentration in n- drift region, the doping concentration $N_{N-}$ is assumed to be $6\times 10^{15}$ $cm^{-3}$.

5) The recombination parameters $h_n$ and $h_p$ control the carrier charge in the carrier storage region, and the amount of carrier charge in the drift region is smaller with

higher recombination parameters. An initial estimate of $10^{-14}cm^4/s$ is made for both recombination parameter $h_n$ and $h_p$.

### 3.5.2 Refinement of Parameter Values

The switching loop parasitic inductance $L_s$ is estimated from the di/dt measurement.

$$L_s = \frac{V_{dc}}{di/dt} \qquad \text{Equation 3-40}$$

With the values of $Q_{rr}$ and $I_F$ obtained from switching tests, the high-level minority carrier lifetime $\tau$ is refined. The high-level minority carrier lifetime $\tau$ is the critical parameter affecting the reverse recovery current waveforms. A better match can be achieved by refinement of high-level minority carrier lifetime $\tau$. After this, the low-doped drift region width $W_{N-}$ and doping concentration $N_{N-}$ can be altered to improve the matching of diode voltage waveforms.

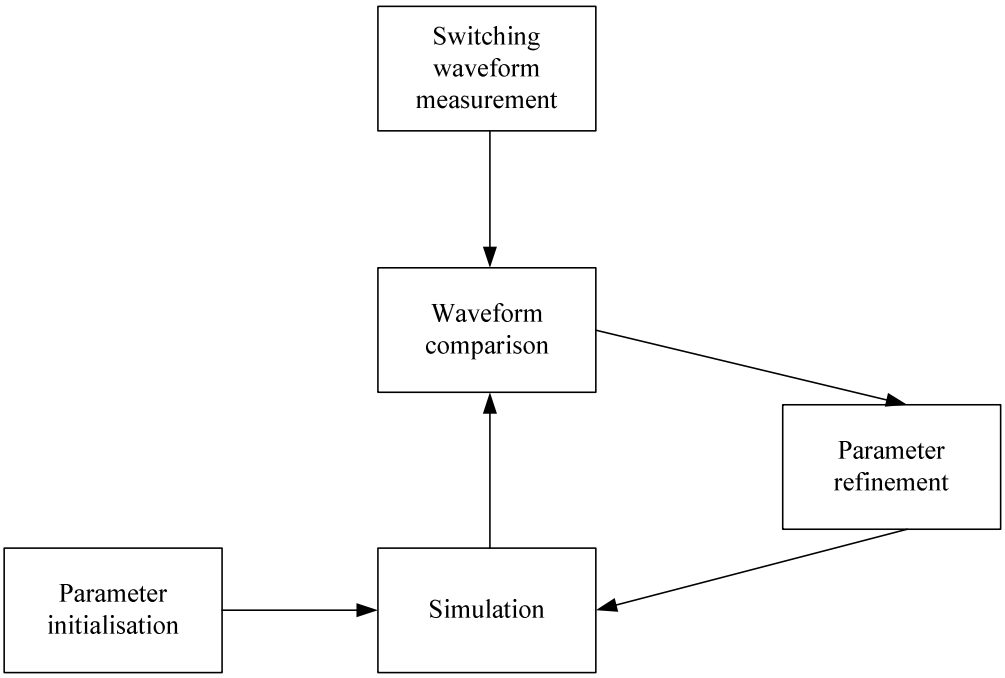



Figure 3.30 The procedure of parameter extraction

### 3.5.3 TEMPERATURE DEPENDENCE

Some parameters in the body diode model are temperature-dependent. These temperature-dependent parameters include: high level minority carrier lifetime $\tau$, electron mobility $\mu_n$, hole mobility $\mu_p$, and intrinsic carrier concentration $n_i$.

The temperature dependent equation for high level minority carrier lifetime $\tau$ is given by:

$$\tau = \tau_0 (\frac{T}{300})^{1.5} \qquad \text{Equation 3-41}$$

where $\tau_0$ is high level minority carrier lifetime at room temperature (300 K).

The electron mobility $\mu_n$ with temperature dependence is given by:

$$\mu_n = \mu_{n0} (\frac{300}{T})^{2.7} \qquad \text{Equation 3-42}$$

where $\mu_{n0}$ is electron mobility at room temperature (300 K).

The hole mobility $\mu_p$ with temperature dependence is given by:

$$\mu_p = \mu_{p0} (\frac{300}{T})^{2.7} \qquad \text{Equation 3-43}$$

where $\mu_{p0}$ is hole mobility at room temperature (300 K).

The intrinsic concentration $n_i$ with temperature dependence is given by:

$$n_i = 1.70 \times 10^{16} T^{1.5} / \exp(\frac{20800}{T}) \qquad \text{Equation 3-44}$$

The junction temperature during operation is determined using thermal RC equivalent circuit as shown in Fig 3.31. The junction temperature calculated from the thermal equivalent circuit is used to update temperature-dependent parameters in the model. The new values of temperature-dependent parameters are used to calculated body diode current and voltage.

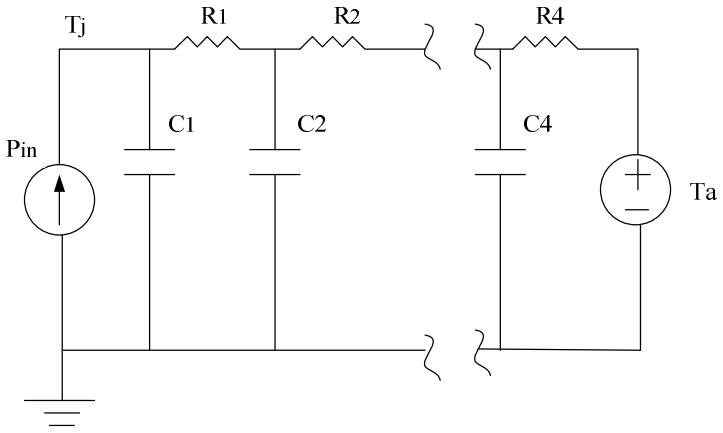



Figure 3.31 Equivalent circuit used for thermal modeling

## 3.6 Model Validation

In this section, the extracted gate-to-source switching loop and drain-to-source switching loop parasitic inductance of the PCB layout are used in Pspice simulation together with SiC MOSFET model and SiC MOSFET body diode model to validate the device model for SiC MOSFET body diode. The SiC MOSFET model used in simulation is from the manufacturer CREE Inc., and the parasitic inductances of the PCB layout are extracted using FastHenry, which is a finite difference software tool for PCB parasitic element extraction. Fig 3.32 shows the simulation circuit, including the extracted parasitic elements (red).

Table 3.2 lists the parameter values for SiC MOSFET (C2M0080120D) body diode model, which are extracted using the parameter extraction method in Section 3.5.

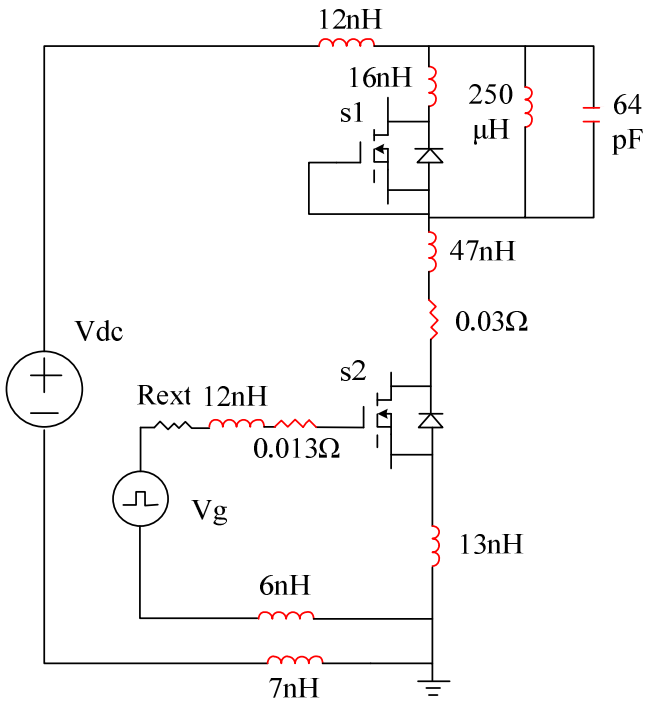



Figure 3.32 Equivalent circuit used for inductive switching

Table 3.2 Extracted model parameter values for SiC MOSFET body diode

| Symbol | Description | Value |
|---|---|---|
| A ($cm^2$) | Chip active area | 0.09 |
| τ (μs) | High-level minority carrier lifetime | 0.021 |
| $W_{N-}$ (μm) | Drift region width | 100 |
| $N_{N-}$ ($cm^{-3}$) | Doping concentration in drift region | $6\times10^{5}$ |
| $h_p$ ($cm^4/s$) | Recombination parameter in P region | $1\times10^{-16}$ |
| $h_n$ ($cm^4/s$) | Recombination parameter in n+ region | $1\times10^{-16}$ |

Fig 3.33 shows the comparison of body diode turn-off voltage and current waveforms between experiment (solid line) and simulation (dashed line) at room temperature 25ºC. The DC supply voltage is 500V, and forward conduction current of

body diode is 30A. The results illustrate a very good matching between simulation and experiment. In the experimental diode voltage waveform, the diode voltage starts increasing and reaches a small value (about 40V) before the diode current reaches the reverse peak current. This voltage drop is caused by parasitic inductances from PCB layout and device packages. The diode begins to block reverse voltage when diode current reaches the reverse peak current.

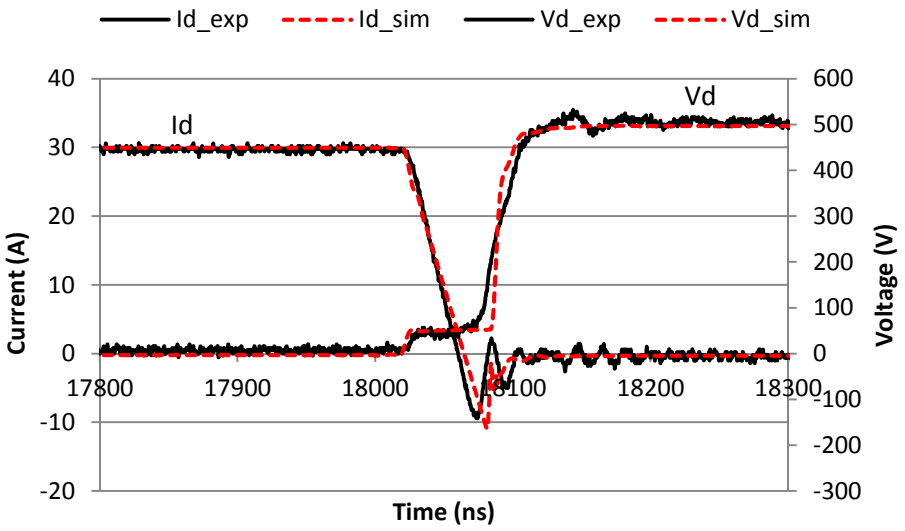



Figure 3.33 The comparison of diode turn-off voltage and current waveforms between experiment (solid) and simulation (dashed) at 25°C

Fig 3.34 illustrates the comparison of body diode turn-off voltage and current waveforms between experiment (solid line) and simulation (dashed line) at 150°C. The DC supply voltage is 500V, and forward conduction current of body diode is 30A. A good matching between experiment and simulation proves the accuracy of the model over a wide temperature range.

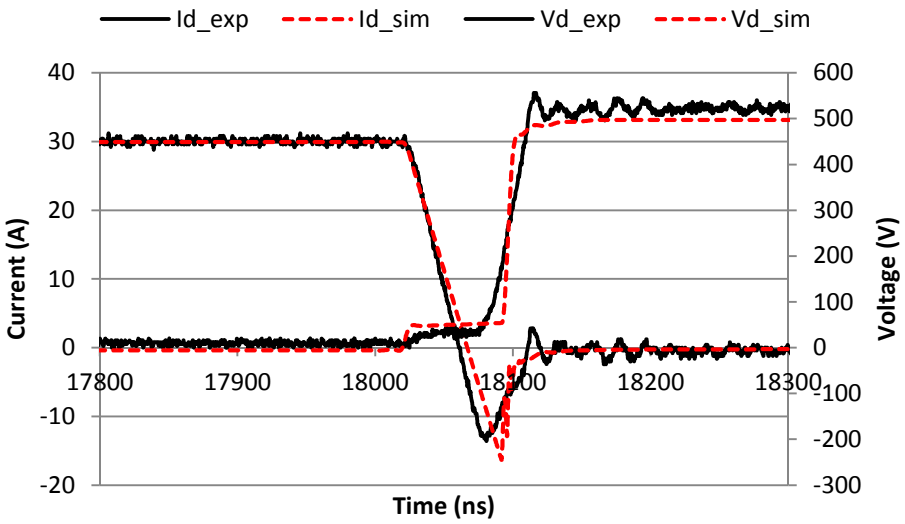



Figure 3.34 The comparison of diode turn-off voltage and current waveforms between experiment (solid) and simulation (dashed) at 150°C

## 3.7 SUMMARY

In this chapter, the static and dynamic characterizations of SiC MOSFET body diode are presented. To my knowledge, this is the first complete characterization of SiC MOSFET body diode in the literature. The static characterization of SiC MOSFET body diode is carried out using a curve tracer. The I-V curves of SiC MOSFET's body diode at varied junction temperatures are given. The dynamic characteristics of SiC MOSFET body diode are tested based on a double pulse test bench. The switching behavior of SiC MOSFET body diode at different current commutating slopes, forward conduction currents and junction temperatures is demonstrated. The device model of body diode is described in detail. The parameter extraction procedure for this model is introduced, which only requires data from the manufacturer's datasheets and one simple switching

measurement. Finally, the comparison between simulation and experiment proves the accuracy of the body diode model and the parameter extraction method.

# CHAPTER 4

# ANALYTICAL LOSS MODEL FOR POWER CONVERTERS WITH SIC MOSFET AND SIC SCHOTTKY DIODE PAIR

Power semiconductor devices realized using wide bandgap semiconductor materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), provide significant performance improvement over traditional Silicon devices. On-state resistance of these new devices is much lower than that of their silicon counterparts for the same die area. Furthermore, wide bandgap devices have much lower device capacitances, which enable them to switch faster. The overall size of a given power converter is expected to be reduced by using these new power semiconductor devices.

Power losses in power semiconductor devices consist of conduction loss and switching loss. The conduction loss can be accurately estimated from the device static I-V characteristics. The switching loss is dependent not only on device parameters, but also on circuit parameters, such as gate drive current, stray inductances and device parasitic capacitances [61][62][63]. For switching loss estimation, the simplest analytical loss model treats power switch turn-on and turn-off current and voltage waveforms as piecewise linear. This model, referred to as the conventional loss model in this chapter, is used as a benchmark to make comparisons with the proposed loss model. The conventional loss model yields closed form equations that can be easily used to calculate device switching loss. However, this model does not take into account parasitic elements

from PCB layout and devices packages. Therefore, the loss prediction based on piecewise linear loss model is not accurate and does not match experimental results very well, especially for high frequency switching operation. In order to improve the accuracy of the analytical loss model, parasitic inductances in circuit and device capacitances should be considered. This is the motivation for the proposed model.

In this chapter, a simple and accurate analytical loss model for Silicon Carbide (SiC) power devices is proposed. A novel feature of this loss model is that it considers the package and PCB parasitic elements in the circuits, nonlinearity of device junction capacitance and ringing loss. The proposed model identifies the switching waveform subintervals, and develops the analytical equations in each switching subinterval to calculate the switching loss. Inductive turn-on and turn-off are thoroughly analyzed. A double pulse test-bench is built to characterize inductive switching behavior of the SiC devices. The analytical results are compared with experimental results. The results show that the proposed loss model can predict switching loss more accurately than the conventional loss model.

## 4.1 Proposed Analytical Loss Model

Power semiconductor device losses consist of two components: conduction loss and switching loss. The conduction loss calculation in MOSFETs and diodes is usually straightforward. Device conduction loss is calculated from the static I-V characteristic. Therefore, the loss analysis in this chapter will focus on switching loss.

In the proposed analytical power loss model, the switching power losses of power semiconductor devices are estimated from their switching waveforms. Fig 4.1 shows the

equivalent circuit for inductive switching of SiC MOSFET and SiC Schottky diode used to estimate the switching loss [64].

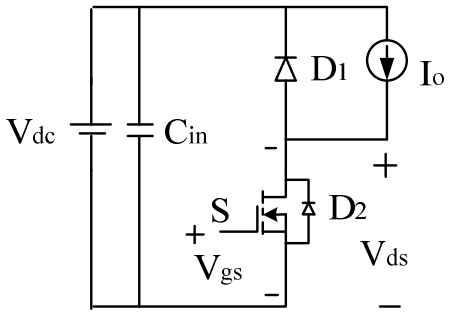



Figure 4.1 Test circuit schematic

In Fig 4.1, switch S is SiC MOSFET, $D_2$ is SiC MOSFET internal body diode, and $D_1$ is SiC Schottky diode. The input is a constant DC voltage source $V_{dc}$, and output is represented by a constant DC load current $I_o$. The gate signal of Switch S is assumed to commutate between $V_{dr\_L}$ and $V_{dr\_H}$. Usually, a slightly negative voltage at turn-off (-5V~-2V) is applied to the gate, while a positive voltage (15V~20V) is used at turn-on. Given the modest transconductance of SiC MOSFETs, the positive voltage is usually at least 18V to reduce conduction losses. In order to analyze the switching transitions with accuracy, Fig 4.2 shows the equivalent circuit with device capacitances and parasitic inductances. $L_1$, $L_2$, $L_3$, $L_{d2}$, $L_{s2}$ and $L_4$ are lumped parasitic inductances extracted from device packages and PCB traces. Parasitic elements of the MOSFET that are considered are gate-source capacitance $C_{gs}$, gate-drain capacitance $C_{gd}$ and drain-source capacitance $C_{ds}$. Due to the nonlinearity of $C_{gd}$ and $C_{ds}$, these capacitances are represented as having a step-wise characteristic with two different values as a function of drain-source voltage, as shown in Fig 4.3 [65]. When $V_{ds}$ is greater than $V_{gs}$-$V_{th}$, $C_{gd}$=$C_{gd1}$ and $C_{ds}$=$C_{ds1}$. When $V_{ds}$ is equal to or less than $V_{gs}$-$V_{th}$, $C_{gd}$=$C_{gd2}$ and $C_{ds}$=$C_{ds2}$. $C_L$ is the load inductor

equivalent parallel capacitance, and $C_{d1}$ is the equivalent junction capacitance of SiC Schottky diode. $R_L$ is the load inductor DC resistance.

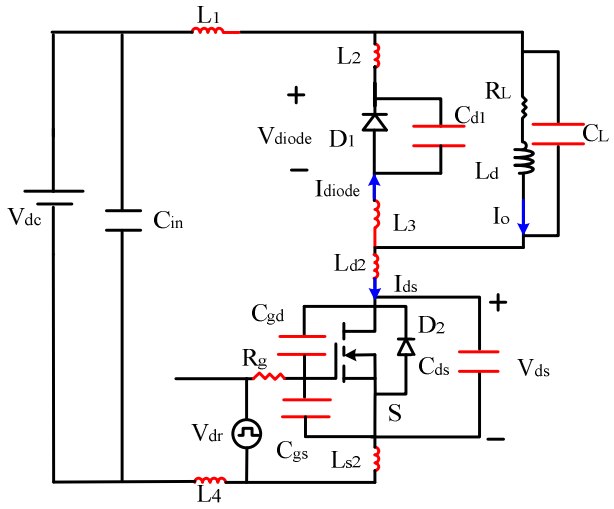



Figure 4.2 Circuit with parasitic inductances and capacitances

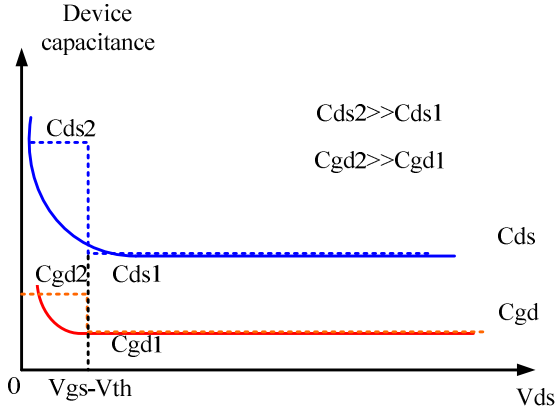



Figure 4.3 Nonlinear capacitances $C_{gd}$ and $C_{ds}$ as a function of drain source voltage $V_{ds}$

Key waveforms during the switching transitions are shown in Fig 4.4 for turn-on and in Fig 4.7 for turn-off. In these figures $V_{dr}$ is the gate driver output voltage, $V_{gs}$ is the gate-source voltage of the SiC MOSFET, $V_{ds}$ is the drain-source voltage of the SiC MOSFET, $I_{ds}$ is the SiC MOSFET drain current, $I_{ch}$ is the SiC MOSFET channel current, $I_{diode}$ is the SiC Schottky diode current, and $V_{diode}$ is the cathode-anode voltage of SiC Schottky diode. The switching waveforms of the power semiconductor devices can be

divided into several time intervals based on their physical behavior. In the following, derivations of the loss model for the turn-on and turn off are presented.

### 4.1.1 MOSFET TURN ON TRANSITION

The switch transition starts at time $t_0$, when SiC Schotty diode $D_1$ is on and is conducting the entire inductive load current. SiC MOSFET S is off and the drain-source voltage is $V_{dc}+V_d$, where $V_d$ is the Schottky diode $D_1$ on-state voltage drop and $V_{dc}$ is the input DC voltage. Fig 4.4 illustrates the turn-on switching waveforms, which will be thoroughly analyzed in the following.

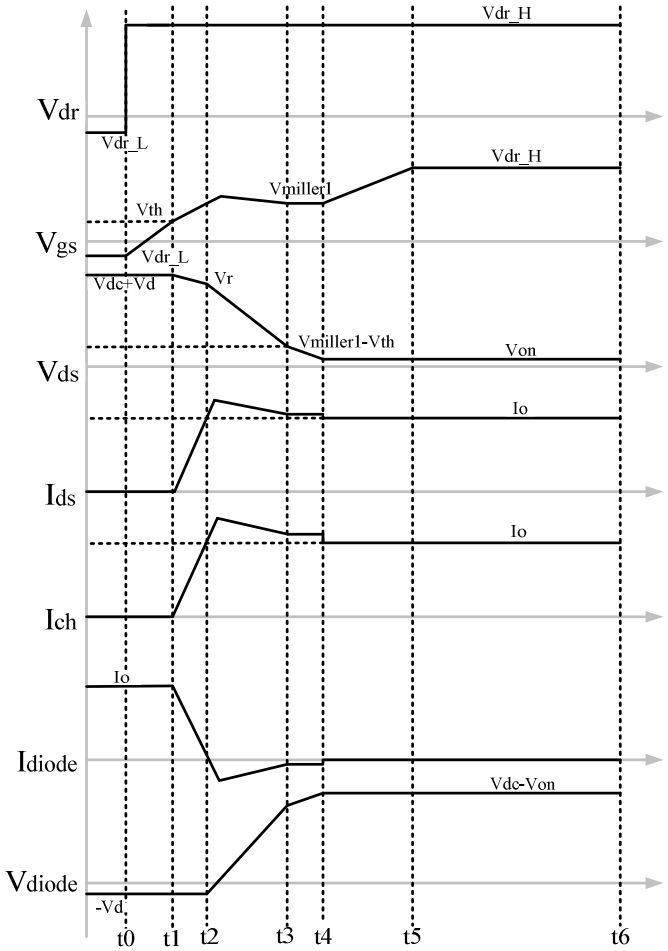



Figure 4.4 Key waveforms of turn-on switching transition

***Stage 1 [$t_0$, $t_1$] turn-on delay time:*** At time $t_0$ the gate signal $V_{dr}$ commutates from $V_{dr\_L}$ to $V_{dr\_H}$. As a result, the gate-source voltage of the MOSFET starts rising, but the MOSFET remains in cutoff until the gate-source voltage reaches the MOSFET threshold voltage $V_{th}$ at time $t_1$. The load current still circulates through SiC Schottky diode $D_1$. No switching loss is generated in this time period. Since the stage does not influence the drain current, the effect of parasitic inductance $L_{s2}$ in the circuit can be neglected and the gate-source voltage is given by:

$$V_{gs}(t) = (V_{dr\_H} - V_{dr\_L})[1 - e^{-(t-t_0)/\tau_{iss}}] + V_{dr\_L} \qquad \text{Equation 4-1}$$

where $\tau_{iss} = R_g(C_{gs} + C_{gd1})$, $C_{gd1}$ is the gate-drain capacitance at high drain-source voltage, $R_g$ is the gate resistance, $V_{dr\_H}$ and $V_{dr\_L}$ are high level gate drive voltage and low level gate drive voltage, respectively. This interval ends at time $t_1$, the instant when $V_{gs}(t_1)=V_{th}$.

***Stage 2 [$t_1$, $t_2$] current rise time:*** In this interval, $V_{gs}$ exceeds $V_{th}$, and the drain current $I_{ds}$ starts increasing from zero to the value of inductive load current $I_o$. During this interval the drain-source voltage is decreased as a result of parasitic inductance voltage drop, due to high di/dt in the circuit. At time $t_2$, the Schottky diode $D_1$ current drops to zero. The drain current is given by:

$$I_{ds}(t) = g_{fs}[V_{gs}(t) - V_{th}] \qquad \text{Equation 4-2}$$

where $g_{fs}$ is the trans-conductance of the SiC MOSFET.

The duration time of this period is given by:

$$t_2 - t_1 = \frac{C_{iss}(V_{miller1} - V_{th})}{I_{g2}} = \frac{I_o C_{iss}}{g_{fs} I_{g2}} \qquad \text{Equation 4-3}$$

where input capacitance $C_{iss} = C_{gs} + C_{gd1}$, $I_{g2}$ is the average gate driving current in stage 2, and $I_o$ is the inductive load current.

The gate-source plateau voltage is given by:

$$V_{miller1} = V_{th} + I_o / g_{fs} \qquad \text{Equation 4-4}$$

The average gate drive current $I_{g2}$ in this stage is given by:

$$I_{g2} = \frac{V_{dr\_H} - 0.5(V_{miller1} + V_{th}) - L_{s2} di_{ds}/dt}{R_g} = \frac{V_{dr\_H} - 0.5(V_{miller1} + V_{th}) - L_{s2} I_o/(t_2 - t_1)}{R_g} \qquad \text{Equation 4-5}$$

where $L_{s2}$ is the common source inductance value, and $R_g$ is the gate resistance. Fig 4.5 shows the equivalent MOSFET driving circuit, and Fig 4.6 shows the gate-source signal waveform. The average gate-source voltage is assumed to be $(V_{miller1}+V_{th})/2$ in stage 2 $[t_1, t_2]$.

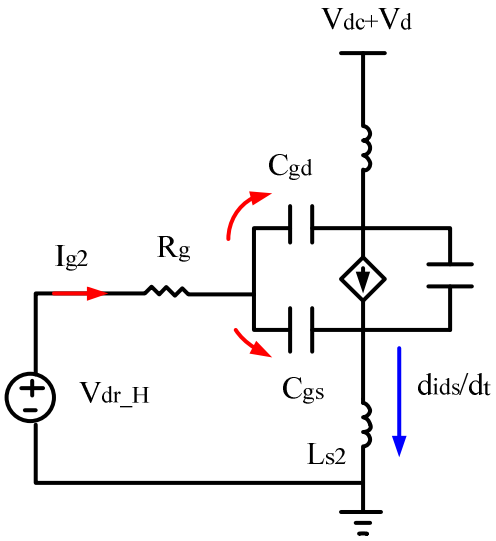



Figure 4.5 MOSFET gate driving equivalent circuit during interval 2 $[t_1, t_2]$

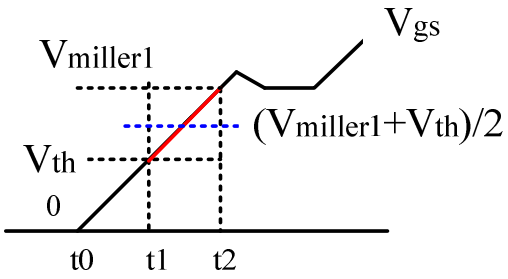



Figure 4.6 Gate-source signal during interval 2 [$t_1$, $t_2$]

The time period $t_2$-$t_1$ is solved by using equations (4-3) and (4-5) as follows:

$$t_2 - t_1 = \frac{C_{iss} R_g I_o + L_{s2} g_{fs} I_o}{(V_{dr\_H} - 0.5V_{th} - 0.5V_{miller1}) g_{fs}} \qquad \text{Equation 4-6}$$

The MOSFET drain-source voltage is decreased by the inductive voltage drop of the stray inductance in the main circuit loop $L_S$ (=$L_1$+$L_2$+$L_3$+$L_4$+$L_{d2}$+$L_{s2}$) and is described as follows:

$$V_{ds}(t) = V_{dc} + V_d - L_s \frac{di_{ds}}{dt} \qquad \text{Equation 4-7}$$

At t=$t_2$, MOSFET drain-source voltage $V_{ds}(t_2)$=$V_r$.

$$V_{ds}(t_2) = V_r = V_{dc} + V_d - L_s \frac{I_o}{(t_2 - t_1)} \qquad \text{Equation 4-8}$$

The total switching energy loss during this period [$t_1$, $t_2$] is

$$E_{1\_2} = \frac{(t_2 - t_1) I_o (V_{dc} + V_d)}{2} - \frac{(t_2 - t_1) I_o (V_{dc} + V_d - V_r)}{3} = \frac{(t_2 - t_1) I_o (V_{dc} + V_d)}{2} - \frac{I_o^2 L_s}{3} \qquad \text{Equation 4-9}$$

***Stage 3 [$t_2$, $t_3$] voltage fall time I:*** At time $t_2$, the SiC MOSFET takes over the total inductive load current and starts to discharge the MOSFET output capacitance $C_{oss}$. The MOSFET drain-source voltage decreases in this time period. The SiC Schottky diode exhibits almost no reverse recovery effects, but its junction capacitance introduces a

small reverse current. The reverse capacitive current causes additional switching power loss in the MOSFET. At time $t_3$, MOSFET drain-source voltage $V_{ds}$ reaches the boundary voltage $V_{miller1}$-$V_{th}$.

The average gate drive current $I_{g3}$ in stage 3 [$t_2$, $t_3$] is:

$$I_{g3} = \frac{V_{dr\_H} - V_{miller1} - [(C_{d1} + C_L)(V_{dc} + V_d - V_{miller1} + V_{th})] / [g_{fs}(t_3 - t_2)]}{R_g} \qquad \text{Equation 4-10}$$

The drain-source voltage $V_{ds}$ in stage 3 [$t_2$, $t_3$] decreases with a large slope dv/dt, which is given by:

$$\frac{dV_{ds}}{dt} = -\frac{I_{g3}}{C_{gd}} = \frac{V_{miller1} - V_{th} - V_r}{t_3 - t_2} \qquad \text{Equation 4-11}$$

where gate drain capacitance $C_{gd}$= $C_{gd1}$.

By substituting (4-10) into (4-11), the time duration of this period [$t_2$, $t_3$] is estimated as:

$$t_3 - t_2 = \frac{(V_r - V_{miller1} + V_{th})C_{gd}R_g + (C_{d1} + C_L)(V_{dc} + V_d - V_{miller1} + V_{th}) / g_{fs}}{V_{dr\_H} - V_{miller1}} \qquad \text{Equation 4-12}$$

where gate drain capacitance $C_{gd}$= $C_{gd1}$.

The total loss in this period, including voltage-current overlap loss and output capacitance discharging loss, is given by:

$$E_{2\_3} = \int_{t2}^{t3} I_{ch}V_{ds}dt = \frac{(t_3 - t_2)(V_r + V_{miller1} - V_{th})}{2} I_o + \frac{1}{2}(C_{d1} + C_L)(V_{dc} + V_d - V_{miller1} + V_{th})(V_r + V_{miller1} - V_{th})$$
$$+ \frac{1}{2}C_{oss1}(V_r - V_{miller1} + V_{th})(V_r + V_{miller1} - V_{th})$$

Equation 4-13

Where $C_{d1}$ is the Schottky diode equivalent capacitance, $C_{oss1}$ is the MOSFET output capacitance at high voltage level and $C_L$ is the load inductor equivalent parallel capacitance.

The MOSFET output capacitance $C_{oss1}$ tends to make the measured drain current $I_{ds}$ deviate from the MOSFET channel current $I_{ch}$, therefore the measured loss in period [$t_2$, $t_3$] is given by:

$$E_{2\_3(measured)} = \int_{t2}^{t3} I_{ds} V_{ds} dt = \frac{(t_3 - t_2)(V_r + V_{miller1} - V_{th})}{2} I_o + \frac{1}{2}(C_{d1} + C_L)(V_{dc} + V_d - V_{miller1} + V_{th})(V_r + V_{miller1} - V_{th}) \quad \text{Equation 4-14}$$

Because the loss due to the discharging of the MOSFET output capacitance cannot be measured, being internal to the MOSFET.

***Stage 4 [$t_3$, $t_4$] voltage fall time II:*** At time $t_3$, the SiC MOSFET goes into the ohmic region. $C_{gd2}$ is the gate-drain capacitance in ohmic region, and $C_{ds2}$ is the drain-source capacitance in the ohmic region. $V_{on}$ is the MOSFET on-state voltage drop. The drain-source voltage $V_{ds}$ continues to fall until it reaches the on-state voltage $V_{on}$.

The average gate drive current $I_{g4}$ in stage 4 [$t_3$, $t_4$] is:

$$I_{g4} = \frac{V_{dr\_H} - V_{miller1}}{R_g} \quad \text{Equation 4-15}$$

The drain-source voltage $V_{ds}$ in stage 4 [$t_3$, $t_4$] decreases with a smaller slope dv/dt, which is given by:

$$\frac{dV_{ds}}{dt} = -\frac{I_{g4}}{C_{gd}} = \frac{V_{on} - V_{miller1} + V_{th}}{t_4 - t_3} \quad \text{Equation 4-16}$$

where gate-drain capacitance $C_{gd} = C_{gd2}$.

By substituting (4-15) into (4-16), the time duration of this period [$t_3$, $t_4$] is estimated as:

$$t_4 - t_3 = \frac{(V_{miller1} - V_{th} - V_{on}) C_{gd} R_g}{V_{dr\_H} - V_{miller1}} \quad \text{Equation 4-17}$$

where gate-drain capacitance $C_{gd}= C_{gd2}$.

The total loss, including voltage-current overlap loss and output capacitance discharging loss, is given by:

$$E_{3\_4} = \int_{t3}^{t4} I_{ch} V_{ds} dt = \frac{(t_4 - t_3)(V_{miller1} - V_{th} + V_{on})}{2} I_o + \frac{1}{2} C_{oss2} (V_{miller1} - V_{on} - V_{th})(V_{miller1} + V_{on} - V_{th})$$
$$+ \frac{1}{2} (C_{d1} + C_L)(V_{miller1} - V_{on} - V_{th})(V_{miller1} + V_{on} - V_{th})$$

Equation 4-18

Where $C_{d1}$ is the Schottky diode equivalent capacitance, $C_{oss2}$ is the MOSFET output capacitance at low voltage level and $C_L$ is the load inductor equivalent parallel capacitance. $V_{on}$ is the MOSFET on-state voltage drop.

The drain current $I_{ds}$ is measured outside the MOSFET, and the measured switching loss in period $[t_3, t_4]$ is given by:

$$E_{3\_4(measured)} = \int_{t3}^{t4} I_{ds} V_{ds} dt = \frac{(t_4 - t_3)(V_{miller1} - V_{th} + V_{on})}{2} I_o$$
$$+ \frac{1}{2} (C_{d1} + C_L)(V_{miller1} - V_{on} - V_{th})(V_{miller1} + V_{on} - V_{th})$$

Equation 4-19

***Stage 5 [$t_4$, $t_5$] gate voltage rise remaining time:*** The gate-source voltage increases exponentially. At time $t_5$, the gate-source voltage reaches to the maximum gate driver voltage $V_{dr\_H}$. No switching loss is generated in this period.

***Stage 6 [$t_5$, $t_6$] MOSFET conduction time:*** The MOSFET is on and it conducts the total inductive load current $I_o$. The MOSFET conduction loss occurs in this time period.

### 4.1.2 MOSFET TURN OFF TRANSITION

The switch transition starts at time $t_6$, when SiC MOSFET S is on and is conducting the entire inductive load current $I_o$. SiC Schottky diode $D_1$ is off and the voltage across cathode and anode is $V_{dc}$-$V_{on}$, where $V_{on}$ is the MOSFET S on-state voltage drop and $V_{dc}$ is the input DC voltage. Fig 4.7 (a) and (b) show the typical turn-off switching waveforms. There are two possible operation modes in turn-off transition: Mode I is the non zero voltage switching (non ZVS) mode and mode II is the ZVS mode.

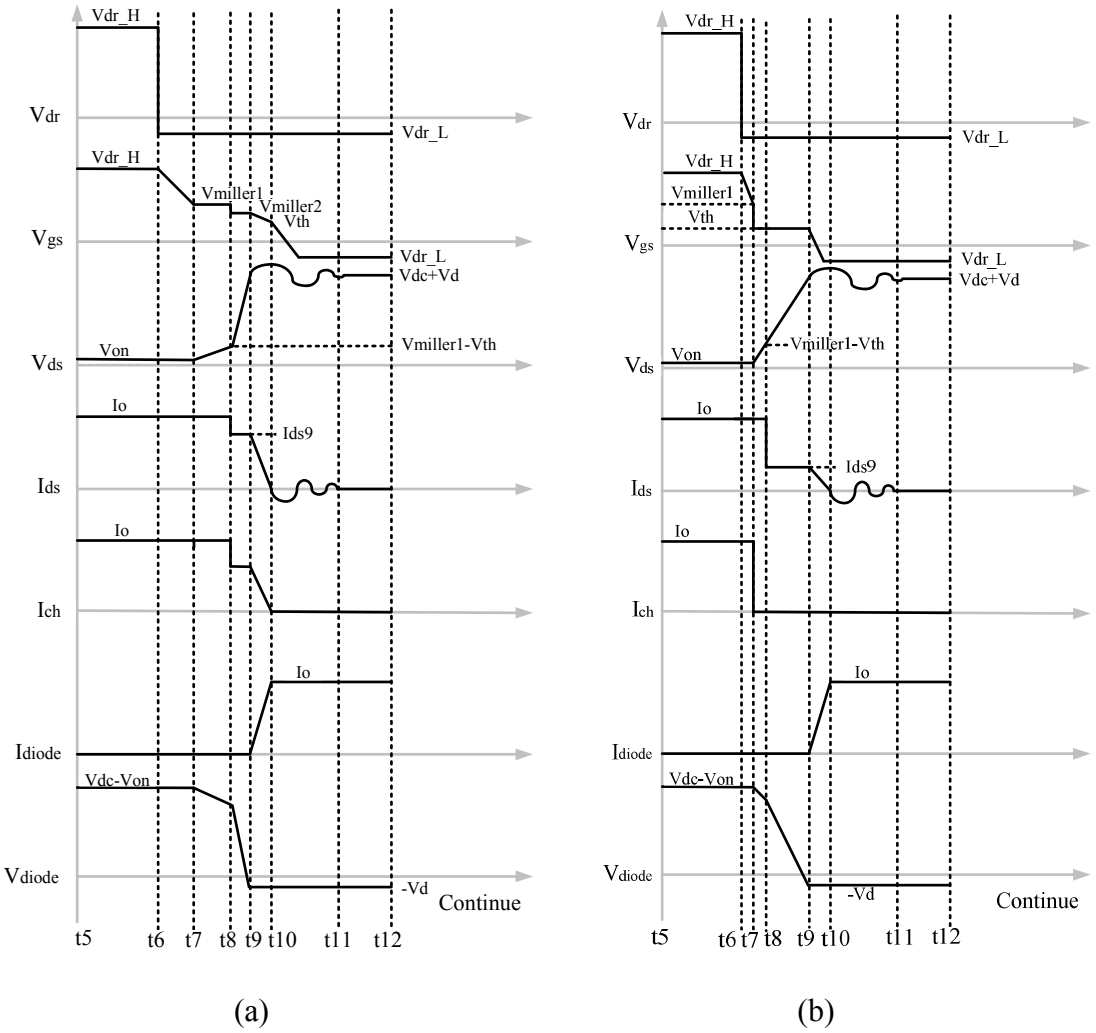



Figure 4.7 Key waveforms of turn-off switching transition (a) Mode I (b) Mode II

***Stage 7 [$t_6$, $t_7$] turn-off delay time:*** The gate signal is set to $V_{dr\_L}$ at time $t_6$, and the MOSFET operates in the ohmic region. $V_{ds}$ will not increase until $V_{gs}$ reduces to $V_{miller1}$. Input capacitance $C_{iss}$ is being discharged through gate drive circuit. The gate source voltage $V_{gs}$ is given by:

$$V_{gs}(t) = (V_{dr\_H} - V_{dr\_L})e^{-(t-t_6)/\tau_{iss}} + V_{dr\_L} \qquad \text{Equation 4-20}$$

where $\tau_{iss} = R_g(C_{gs} + C_{gd2})$, $C_{gd2}$ is the gate-drain capacitance at low drain-source voltage, and $R_g$ is the gate resistance. This interval ends at time $t_7$, when $V_{gs}(t_7)=V_{miller1}$.

***Stage 8 [$t_7$, $t_8$] voltage rise time I:*** There are two possible cases in this period as described in the following:

*Mode I (non ZVS turn-off)*: MOSFET drain-source voltage $V_{ds}$ increases with a smaller slope in this period. In this stage, MOSFET still operates in ohmic region. At time $t_8$, drain-source voltage $V_{ds}$ reaches the boundary voltage $V_{miller1}$-$V_{th}$, and MOSFET transitions to the saturation region. Drain current $I_{ds}$ remains approximately constant and is equal to loading current $I_o$.

The average gate drive current $I_{g8}$ in this time period is given by:

$$I_{g8} = \frac{V_{miller1} - V_{dr\_L}}{R_g} \qquad \text{Equation 4-21}$$

where $V_{miller1}=I_o/g_{fs}+V_{th}$.

The drain-source voltage $V_{ds}$ in stage 8 [$t_7$, $t_8$] increases with a slope dv/dt, which is given by:

$$\frac{dV_{ds}}{dt} = \frac{I_{g8}}{C_{gd}} = \frac{V_{miller1} - V_{th} - V_{on}}{t_8 - t_7} \qquad \text{Equation 4-22}$$

where gate-drain capacitance $C_{gd}= C_{gd2}$.

By substituting (4-21) into (4-22), the time duration of this period [$t_7$, $t_8$] is estimated as:

$$t_8 - t_7 = \frac{(V_{miller1} - V_{th} - V_{on})C_{gd}R_g}{V_{miller1} - V_{dr\_L}} \qquad \text{Equation 4-23}$$

where gate-drain capacitance $C_{gd}$= $C_{gd2}$.

The total loss, considering voltage-current overlap and capacitance charging, is given by:

$$E_{7\_8} = \int_{t7}^{t8} I_{ch}V_{ds}dt = \frac{(t_8 - t_7)(V_{miller1} - V_{th} + V_{on})}{2} I_o - \frac{1}{2}C_{oss2}(V_{miller1} - V_{on} - V_{th})(V_{miller1} + V_{on} - V_{th})$$

Equation 4-24

Where $C_{oss2}$ is the MOSFET output capacitance at low voltage level and $V_{on}$ is MOSFET on-state voltage drop.

The measured switching loss during this period [$t_7$, $t_8$] is given by:

$$E_{7\_8(measured)} = \int_{t7}^{t8} I_{ds}V_{ds}dt = \frac{(t_8 - t_7)(V_{miller1} - V_{th} + V_{on})}{2} I_o \qquad \text{Equation 4-25}$$

*Mode II (ZVS turn-off)*: The MOSFET drain-source voltage $V_{ds}$ increases in this period, which is shown in Fig 4.7 (b). The measured drain current $I_{ds}$ remains approximately constant and is equal to the loading current $I_o$, and a very small capacitive current charging Schottky diode junction capacitance $C_{d1}$ and load inductor capacitance $C_L$ is neglected in this period. The gate-source voltage $V_{gs}$ decreases from the miller voltage $V_{miller1}$ to threshold voltage $V_{th}$ at time $t_7$, and remains equal to $V_{th}$ in period [$t_7$, $t_8$]. The MOSFET channel current drops to zero, and drain-source voltage $V_{ds}$ increases from on-state voltage $V_{on}$ to $V_{miller1}$-$V_{th}$.

The average gate drive current $I_{g8}$ in this time period is:

$$I_{g8} = \frac{V_{th} - V_{dr\_L}}{R_g}$$ Equation 4-26

During the interval [$t_7$, $t_8$], drain-source capacitance $C_{ds}$ is charged from $V_{on}$ to $V_{miller1}$-$V_{th}$. As shown in Fig 4.8, gate drive current $I_{g8}$ discharges capacitance $C_{gd}$, and gate drive current $I_{g8}$ is given by:

$$I_{g8} = C_{gd} \frac{V_{miller1} - V_{th} - V_{on}}{t_8 - t_7}$$ Equation 4-27

where gate-drain capacitance $C_{gd}$=$C_{gd1}$.

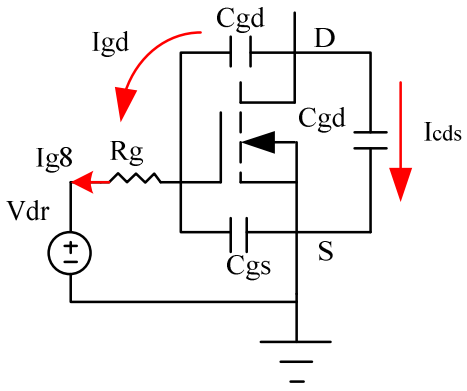



Figure 4.8 MOSFET operation during interval 8 [$t_7$, $t_8$]

By substituting (4-26) into (4-27), the time duration of this period [$t_7$, $t_8$] is given by:

$$t_8 - t_7 = \frac{R_g C_{gd} (V_{miller1} - V_{th} - V_{on})}{V_{th} - V_{dr\_L}}$$ Equation 4-28

where gate-drain capacitance $C_{gd}$ = $C_{gd1}$, and drain-source capacitance $C_{ds}$ =$C_{ds1}$.

The total switching loss in time period [$t_7$, $t_8$] is given by:

$$E_{7\_8} = \int_{t7}^{t8} I_{ch} V_{ds} dt = 0$$ Equation 4-29

The measured switching loss in time period [$t_7$, $t_8$] is given by:

$$E_{7\_8(measured)} = \int_{t7}^{t8} I_{ds} V_{ds} dt = \frac{(t_8 - t_7)(V_{miller1} - V_{th} + V_{on})}{2} I_o \qquad \text{Equation 4-30}$$

***Stage 9 [$t_8$, $t_9$] voltage rise time II:*** The MOSFET drain-source voltage increases in this period. The load inductor parallel capacitance $C_L$ and Schottky diode junction capacitance $C_{d1}$ are discharged by load current. The measured drain current is reduced from load current $I_o$ by capacitances $C_L$ and $C_{d1}$ charging currents.

*Mode I (non ZVS turn-off)*: The average gate drive current $I_{g9}$ in this time period is:

$$I_{g9} = \frac{V_{miller2} - V_{dr\_L}}{R_g} \qquad \text{Equation 4-31}$$

The measured drain current $I_{ds}$ decreases from $I_o$ to $I_{ds9}$, and $I_{ds9}$ is given by:

$$I_{ds9} = I_o - (C_{d1} + C_L)\frac{dV_{ds}}{dt} = I_o - (C_{d1} + C_L)\frac{(V_{dc} - V_{miller1} + V_d + V_{th})}{(t_9 - t_8)} \qquad \text{Equation 4-32}$$

The MOSFET channel current $I_{ch}$ also decreases from $I_o$ to $I_{ch9}$ in this period and $I_{ch9}$ is given by:

$$I_{ch9} = I_{ds9} - (C_{gd} + C_{ds})\frac{dV_{ds}}{dt} = I_{ds9} - (C_{gd} + C_{ds})\frac{(V_{dc} - V_{miller1} + V_d + V_{th})}{(t_9 - t_8)} \qquad \text{Equation 4-33}$$

where gate-drain capacitance is $C_{gd} = C_{gd1}$, drain-capacitance is $C_{ds} = C_{ds1}$.

The voltage $V_{miller2}$ is given by:

$$V_{miller2} = V_{th} + [I_{ds9} - (C_{ds} + C_{gd})(V_{dc} - V_{miller1} + V_d + V_{th})/(t_9 - t_8)]/g_{fs} \qquad \text{Equation 4-34}$$

The increasing slope of drain-source voltage $V_{ds}$ in this time period is given by:

$$\frac{dV_{ds}}{dt} = \frac{I_{g9}}{C_{gd}} = \frac{V_{dc} + V_d - V_{miller1} + V_{th}}{t_9 - t_8} \qquad \text{Equation 4-35}$$

where gate-drain capacitance $C_{gd} = C_{gd1}$.

By putting (4-32)-(4-35) into (4-31), the duration time $t_9$-$t_8$ is given by:

$$t_9 - t_8 = \frac{[C_{gd}R_g + (C_{ds} + C_{gd} + C_{d1} + C_L)/g_{fs}](V_{dc} + V_d - V_{miller1} + V_{th})}{V_{miller1} - V_{dr\_L}}$$

Equation 4-36

The total switching loss in time period [$t_8$, $t_9$] is given by:

$$E_{8\_9} = \int_{t8}^{t9} I_{ch}V_{ds}dt = \frac{(t_9 - t_8)(V_{dc} + V_d + V_{miller1} - V_{th})}{2} I_o - \frac{1}{2}C_{oss1}(V_{dc} + V_d - V_{miller1} + V_{th})(V_{dc} + V_d + V_{miller1} - V_{th})$$
$$-\frac{1}{2}(C_{d1} + C_L)(V_{dc} + V_d - V_{miller1} + V_{th})(V_{dc} + V_d + V_{miller1} - V_{th})$$

Equation 4-37

where $C_{oss1}$ is the MOSFET output capacitance at high voltage level.

The total measured switching loss in time period [$t_8$, $t_9$] is given by:

$$E_{8\_9(measured)} = \int_{t8}^{t9} I_{ds}V_{ds}dt = \frac{(t_9 - t_8)(V_{dc} + V_d + V_{miller1} - V_{th})}{2} I_o$$
$$-\frac{1}{2}(C_{d1} + C_L)(V_{dc} + V_d - V_{miller1} + V_{th})(V_{dc} + V_d + V_{miller1} - V_{th})$$

Equation 4-38

*Mode II (ZVS turn-off)*: The MOSFET drain-source voltage $V_{ds}$ increases from $V_{miller1}$-$V_{th}$ to $V_{dc}$+$V_d$ during the time period [$t_8$, $t_9$]. The Schottky diode voltage $V_{diode}$ decreases from $V_{dc}$-$V_{miller1}$+$V_{th}$ to –$V_d$ during this time period. As shown in Fig 4.9, the MOSFET channel current is zero, and the load current is divided by the device parasitic capacitances.

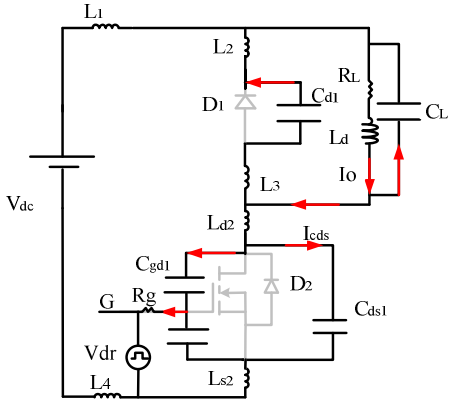



Figure 4.9 Current conduction path during time period [$t_8$, $t_9$] (Mode II)

The capacitive current $I_{cds}$ flowing through the MOSFET drain-source capacitance $C_{ds}$ is given by:

$$I_{cds} = \frac{C_{ds}}{C_{ds} + C_{gd} + C_{d1} + C_L} I_o \qquad \text{Equation 4-39}$$

The capacitive current $I_{cds}$ is also given by:

$$I_{cds} = C_{ds} \frac{dV_{ds}}{dt} = C_{ds} \frac{V_{dc} + V_d - V_{miller1} + V_{th}}{t_9 - t_8} \qquad \text{Equation 4-40}$$

The time period $t_9$-$t_8$ can be obtained from (4-39) and (4-40), and it is given by:

$$t_9 - t_8 = \frac{(V_{dc} + V_d - V_{miller1} + V_{th})(C_{ds} + C_{gd} + C_{d1} + C_L)}{I_o} \qquad \text{Equation 4-41}$$

where gate-drain capacitance $C_{gd}$= $C_{gd1}$, and drain-source capacitance $C_{ds}$= $C_{ds1}$.

The measured drain current $I_{ds}$ is constant in this period and it is given by:

$$I_{ds} = I_o - (C_{d1} + C_L) \frac{dV_{ds}}{dt} = I_o - (C_{d1} + C_L) \frac{(V_{dc} - V_{miller1} + V_{th} + V_d)}{(t_9 - t_8)} \qquad \text{Equation 4-42}$$

The total switching loss $E_{8\_9}$ in time period [$t_8$, $t_9$] is zero, due to zero MOSFET channel current. The total measured switching loss in time period [$t_8$, $t_9$] is given by:

$$E_{8\_9(measured)} = \int_{t8}^{t9} I_{ds} V_{ds} dt = \frac{(t_9 - t_8)(V_{dc} + V_d + V_{miller1} - V_{th})}{2} I_{ds9} \qquad \text{Equation 4-43}$$

where the measured drain current $I_{ds9}$ is obtained from equation (4-42) as $I_{ds9}$=$I_{ds}$($t_9$).

***Stage 10 [t9, t10] Current fall time:*** After the Schottky diode $D_1$ becomes forward-biased at time $t_9$, the current begins to divert from MOSFET to Schottky diode. This interval ends when the drain current becomes zero.

*Mode I (non ZVS turn-off)*: At time $t_{10}$ the gate-source voltage $V_{gs}$ reaches $V_{th}$, and the MOSFET channel current reaches zero. The MOSFET suffers an extra voltage stress,

because decreasing drain current introduces a voltage drop across the parasitic inductances.

The time duration of this period [$t_9$, $t_{10}$] is given by:

$$t_{10} - t_9 = \frac{I_{ds9} C_{iss}}{g_{fs} I_{g10}} \qquad \text{Equation 4-44}$$

where MOSFET input capacitance $C_{iss} = C_{gs} + C_{gd1}$, $I_{g10}$ is the average gate drive current in stage 10, $C_{gd1}$ is the gate-drain capacitance at high drain-source voltage. The measured drain current $I_{ds9}$ is obtained from equation (4-32).

Fig 4.10 shows the equivalent MOSFET drive circuit during stage 10, and Fig 4.11 shows the gate signal waveform in this time period.

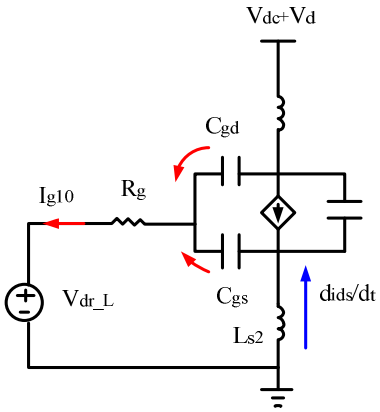



Figure 4.10 MOSFET gate driving equivalent circuit during time period [$t_9$, $t_{10}$]

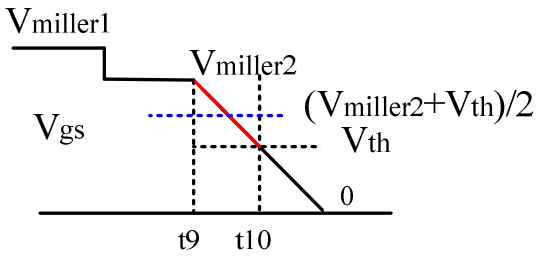



Figure 4.11 Gate signal during time period [$t_9$, $t_{10}$]

The average gate drive current $I_{g10}$ in this time period is:

$$I_{g10} = \frac{0.5(V_{miller2} + V_{th}) - V_{dr\_L} - L_{s2} di_{ds} / dt}{R_g} = \frac{0.5(V_{miller2} + V_{th}) - V_{dr\_L} - L_{s2} I_{ds9} / (t_{10} - t_9)}{R_g} \quad \text{Equation 4-45}$$

where $L_{s2}$ is the common source inductance value. The voltage $V_{miller2}$ is given by equation (4-34).

By substituting (4-45) into (4-44), the duration time $t_{10}$-$t_9$ is given by:

$$t_{10} - t_9 = \frac{R_g I_{ds9} C_{iss} + L_{s2} I_{ds9} g_{fs}}{(0.5V_{miller2} + 0.5V_{th} - V_{dr\_L}) g_{fs}} \quad \text{Equation 4-46}$$

The MOSFET drain-source voltage is increased by an inductive voltage drop due to the high di/dt rate of the current passing through the parasitic inductances in circuit.

$$V_{ds}(t_{10}) = V_{dc} + V_d - L_s \frac{di_{ds}}{dt} = V_{dc} + V_d + L_s \frac{I_{ds9}}{(t_{10} - t_9)} \quad \text{Equation 4-47}$$

where $L_s$ is the stray inductance in the main circuit loop.

The power loss due to the voltage-current overlap is given by:

$$E_{9\_10} = \int_{t9}^{t10} I_{ch} V_{ds} dt = \frac{(t_{10} - t_9)(V_{dc} + V_d)}{2} I_{ch9} + \frac{L_s I_{ds9} I_{ch9}}{2} \quad \text{Equation 4-48}$$

The MOSFET channel current $I_{ch9}$ is obtained from equation (4-33) as $I_{ch9}=I_{ch}(t_9)$.

The measured switching loss in this time period [$t_9$, $t_{10}$] is given by:

$$E_{9\_10(measured)} = \int_{t9}^{t10} I_{ds} V_{ds} dt = \frac{(t_{10} - t_9)(V_{dc} + V_d)}{2} I_{ds9} + \frac{L_s I_{ds9}^2}{2} \quad \text{Equation 4-49}$$

The measured drain current $I_{ds9}$ is obtained from equation (4-32).

*Mode II (ZVS turn-off)*: The gate-source voltage drops to $V_{dr\_L}$ in this time period, and the MOSFET channel current is zero. The resonance between MOSFET output capacitances and circuit parasitic inductances begins at time $t_9$. The resonance period $T_r$ can be approximated by:

$$T_r = 2\pi\sqrt{L_s C_{oss}} \qquad \text{Equation 4-50}$$

where $L_s$ is the main loop parasitic inductance, and MOSFET output capacitance $C_{oss}=C_{oss1}$.

The duration time $t_{10}$-$t_9$ approximately is approximately a quarter of resonance period $T_r$, and it is given by:

$$t_{10} - t_9 = \pi\sqrt{L_s C_{oss}} / 2 \qquad \text{Equation 4-51}$$

The power loss $E_{9\_10}$ due to the voltage-current overlap is zero, because the channel current is zero in this time period.

The measured switching loss in the period [$t_9$, $t_{10}$] is expressed as:

$$E_{9\_10(measured)} = \int_{t9}^{t10} I_{ds} V_{ds} dt \approx \frac{(t_{10} - t_9)(V_{dc} + V_d)}{2} I_{ds9} + \frac{L_s I_{ds9}^2}{2} \qquad \text{Equation 4-52}$$

where the measured drain current $I_{ds9}$ is obtained from equation (4-42) as $I_{ds9}=I_{ds}(t_9)$.

***Stage 11 [$t_{10}$, $t_{11}$] voltage ringing time:*** Drain-source voltage ringing occurs in this time period, due to the resonance between MOSFET output capacitance and stray inductance. Eventually, this high frequency resonance is damped by the stray resistance in the circuit and all the ringing energy is dissipated.

The measured ringing loss during turn-off period [$t_{10}$, $t_{11}$] is given by:

$$E_{10\_11} = \frac{1}{2} Q_{peak} V_{peak} - \frac{1}{2} Q_{V_{dc}+V_d} (V_{dc} + V_d) - V_{dc} (Q_{peak} - Q_{V_{dc}+V_d}) \qquad \text{Equation 4-53}$$

where $V_{peak}$ is the drain-source peak voltage in period [$t_{10}$, $t_{11}$], $Q_{peak}$ is the output capacitor charge when $V_{ds}=V_{peak}$, and $Q_{Vdc+Vd}$ is the output capacitor charge when $V_{ds}=V_{dc}+V_d$.

***Stage 12 [$t_{11}$, $t_{12}$] Diode conduction time:*** The inductive load current $I_o$ flows entirely through the SiC Schottky diode $D_1$. No switching loss occurs in the time period [$t_{11}$, $t_{12}$].

## 4.2 Experimental Verification of The Analytical Loss Model

### 4.2.1 Hardware Setup

In order to verify the analytical loss model, a printed circuit board (PCB) test-bench was built to conduct the inductive switching experiments on SiC power devices including MOSFET and Schottky diode. The parasitic inductances from the PCB layout were minimized, when the PCB was designed. Fig 4.12 shows the experimental setup of inductive switching. The test-bench includes a test socket for SiC MOSFET, a test socket for SiC Schottky diode, gate drive circuit, input capacitor bank, a load inductor, probe-tip-adapters, and a Pearson coil for drain current measurement. Polypropylene film capacitors with very low ESL (equivalent series inductance) are used to provide a low inductance DC voltage source for the test-bench. The MOSFET under test is a SiC MOSFET CMF10120D from CREE Inc. rated at 1200V/24A. A gate driver IC IXDD609SI based on the totem-pole structure from IXYS Corporation is used as the SiC MOSFET gate driver with 9A maximum source/sink drive current [66]. The gate driver output voltage switches from -5V to 18V. The free-wheeling diode under test is a SiC Schottky diode C4D20120A from CREE Inc rated at 1200V/20A. Probe-tip-adapters are used to measure MOSFET's gate-source voltage $V_{gs}$, and drain-source voltage $V_{ds}$. A Pearson coil (model 2878) is used to measure the drain current $I_{ds}$. A 250 μH ferrite-core inductor is used as the load inductor for inductive switching experiments.

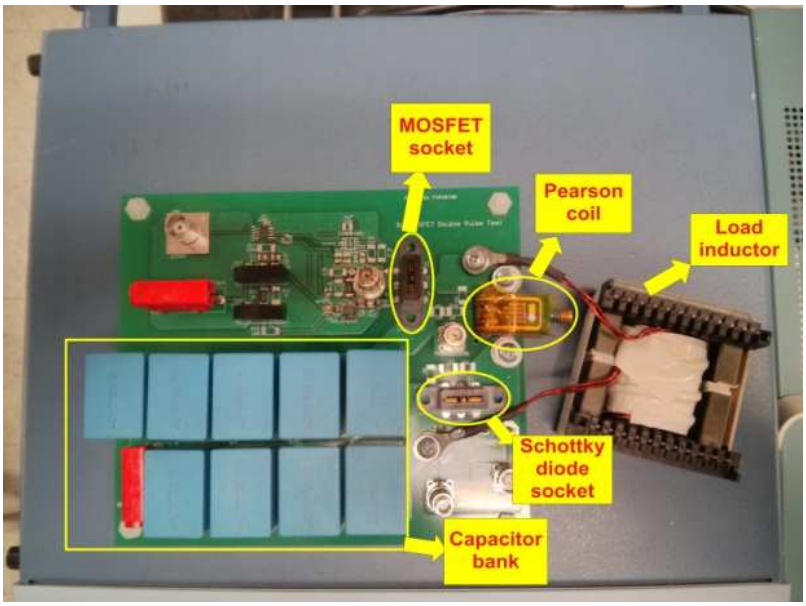



Figure 4.12 Experimental setup of inductive switching tests

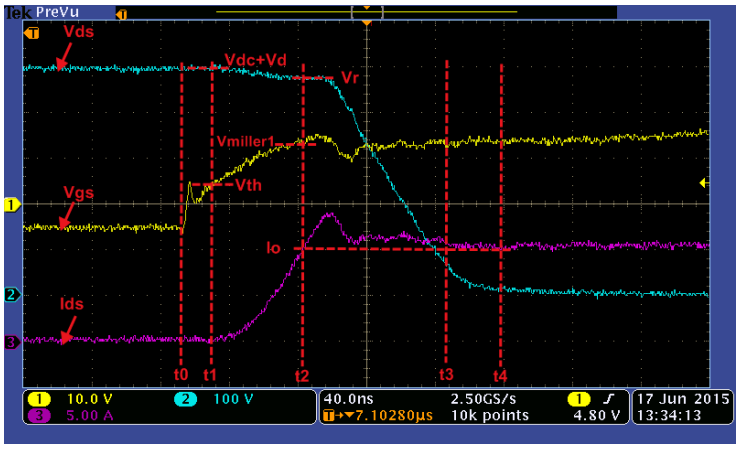
### 4.2.2 PARAMETER EXTRACTION

An inductance extraction software tool FastHenry is used to estimate the parasitic inductances from PCB layout. Device parameter values are extracted from manufacturer's datasheets. Threshold voltage $V_{th}$ and MOSFET transconductance $g_{fs}$ are extracted from device transfer characteristics curve. Drain-source capacitances $C_{ds1}$ and $C_{ds2}$ are obtained from device output capacitance curve as a function of drain-source voltage. Reverse transfer capacitances $C_{gd1}$ and $C_{gd2}$ are extracted from device transfer capacitance curve as a function of drain-source voltage. Gate-source capacitances $C_{gs}$ is obtained from device input capacitance curve.

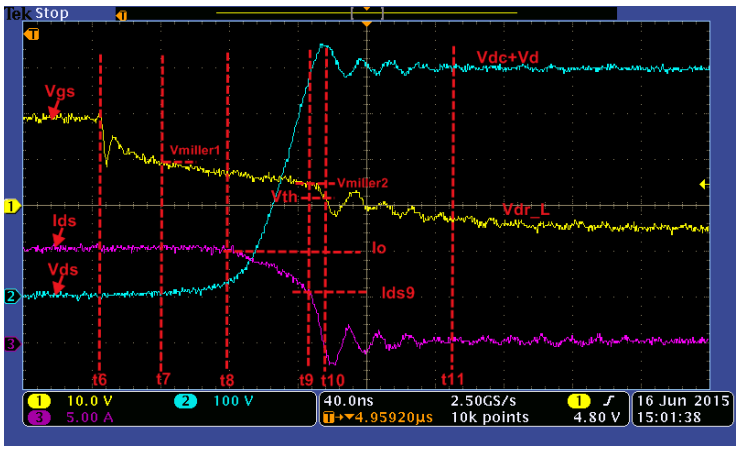
### 4.2.3 SWITCHING WAVEFORMS

The DC input voltage $V_{dc}$ is 500V in experiments. Double pulse switching tests are carried out to study switching waveforms and power losses. The switching

waveforms are measured with a Tektronix high-speed oscilloscope MSO3014 (bandwidth: 500MHz, sampling rate: 2.5GS/s). To correctly measure power losses, probe deskew is carried out before measurement. Fig 4.13 shows turn-on and turn-off transient waveforms (gate-source voltage $V_{gs}$, drain-source voltage $V_{ds}$, and drain current $I_{ds}$) for inductive load switching at 500V input, 10A load current, and 47Ω gate resistance. In the turn-on transition, an overshoot of drain current $I_{ds}$ is observed in the period [$t_2$, $t_3$], due to the Schottky diode reverse capacitive current. The gate source voltage $V_{gs}$ reaches the threshold voltage $V_{th}$, when the drain current $I_{ds}$ decreases to zero at time $t_{10}$. It clearly shows that MOSFET channel current $I_{ch}$ is above zero in [$t_8$, $t_{10}$] and therefore the turn-off transition follows Model I (non ZVS) turn off. Fig 4.14 shows turn-on and turn-off transient waveforms (gate-source voltage $V_{gs}$, drain-source voltage $V_{ds}$, and drain current $I_{ds}$) for inductive load switching at 500V input, 10A load current, and 3.3Ω gate resistance. In the turn-on transition, an overshoot of drain current $I_{ds}$ is also observed in the period [$t_2$, $t_3$], because of the Schottky diode reverse capacitive current. In the turn-off transition, SiC MOSFET operates in Mode II. As seen in Fig 4.14 (b), gate-source voltage $V_{gs}$ reaches the threshold voltage $V_{th}$ at time $t_7$, while the drain current $I_{ds}$ is equal to the load current $I_o$. The MOSFET channel is off after the time $t_7$, and load current flows through the MOSFET output capacitance instead of the MOSFET channel. The MOSFET channel is turned off before the drain-source voltage $V_{ds}$ rises significantly above zero, and turn-off switching loss is small in this case.

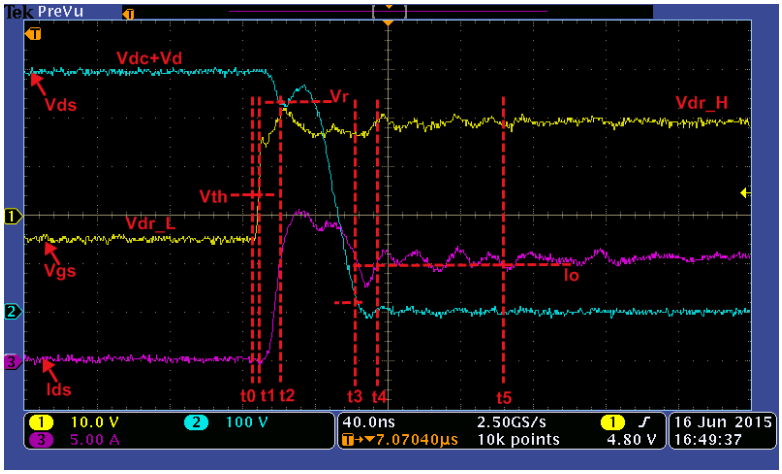



(a)

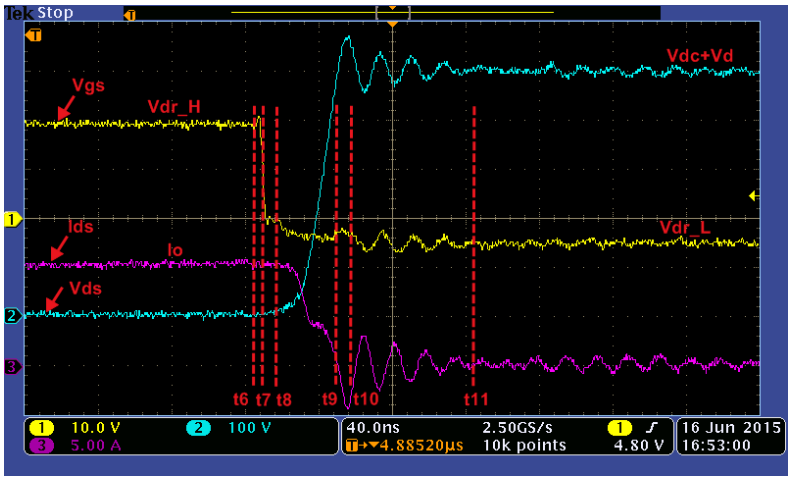



(b)

Figure 4.13 SiC MOSFET switching waveforms (10A load current, 47Ω gate resistance)
(a) turn-on transition (b) turn-off transition




(a)




(b)

Figure 4.14 SiC MOSFET switching waveforms (10A load current, 3.3Ω gate resistance) (b) turn-on transition (b) turn-off transition

The waveforms calculated with the analytical model and experimental waveforms are compared in Fig 4.15, when the load current is 10A and gate resistance is 47Ω. The 3-D inductance extraction software program FastHenry is used to estimate parasitic inductances in the PCB layout [67]. A good matching between analytical and experimental results is observed from Fig 4.15.

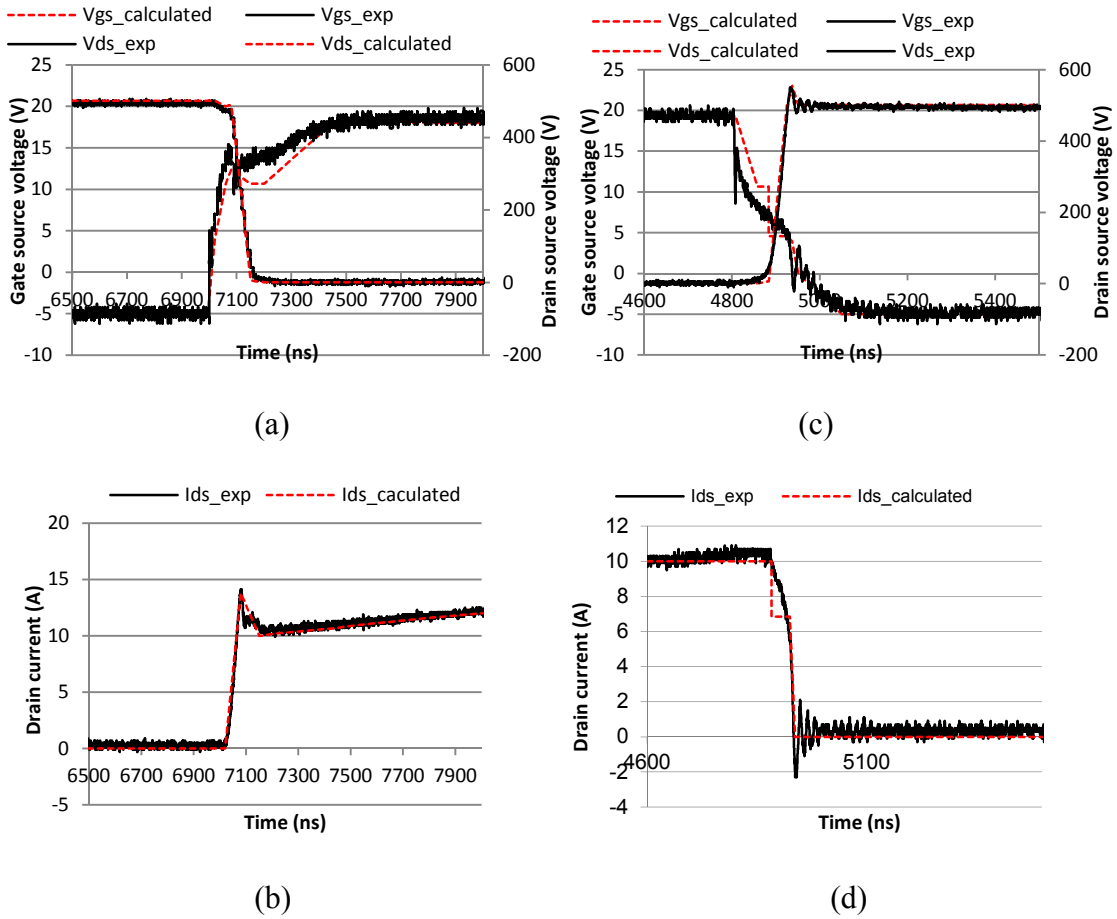



Figure 4.15 Comparison between measured (dark solid lines) and analytical (red dashed lines) waveforms for (a) $V_{gs}$ and $V_{ds}$ at turn-on transition (b) $I_{ds}$ at turn-on transition (c) $V_{gs}$ and $V_{ds}$ at turn-off transition (d) $I_{ds}$ at turn-off transition (10A load current, 47Ω gate resistance)

### 4.2.4 Switching Losses

The DC input voltage $V_{dc}$ is 500V in experimental measurements. Fig 4.16 shows the device measured turn-on switching energy $E_{on}$, turn-off switching energy $E_{off}$ and total switching energy $E_{total}$, as a function of load current $I_o$, when the gate resistance is 14.7 Ω. As the load current increases, the turn-on switching energy and turn-off switching energy increase as well. However, turn-off energy loss $E_{off}$ does not increase as fast as the turn-on switching energy loss $E_{on}$, due to the reduction of turn-off time at a higher load current. Fig 4.17 shows the device turn-on and turn-off times as a function of

load current, when gate resistance is 14.7Ω. The turn-on time increases with load current, by contrast, the turn-off time decreases with load current.

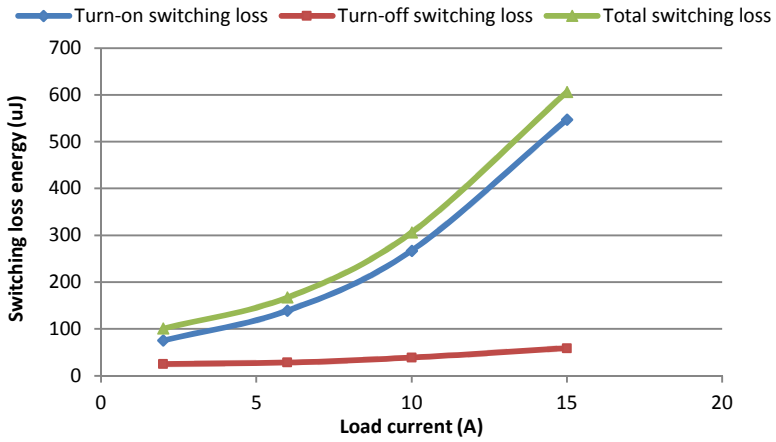



Figure 4.16 Switching energy losses as a function of load current (experimental)

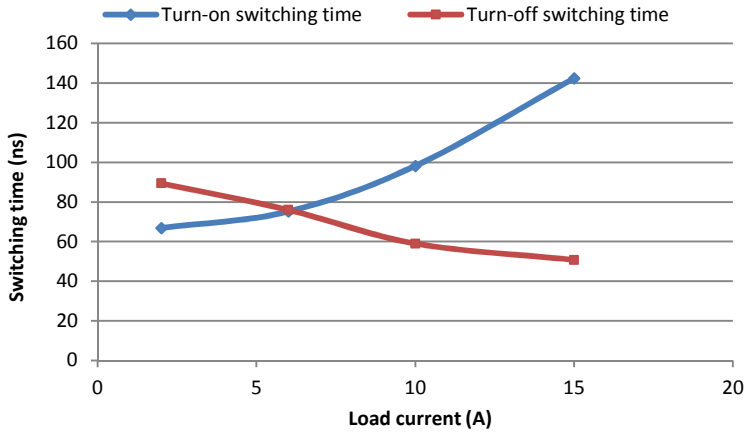



Figure 4.17 Switching times as a function of load current (experimental)

Fig 4.18 shows the device turn-on and turn-off switching energies at 10A load current as a function of the gate resistance. As seen, both the turn-on and turn-off switching loss energies vary approximately linearly with gate resistance. A larger $R_g$ slows down the switching transitions (both voltage and current rates) and, as a result, the switching energy increases. Fig 4.19 shows the device total turn-on and turn-off times as a function of gate resistance, when load current is 10A.

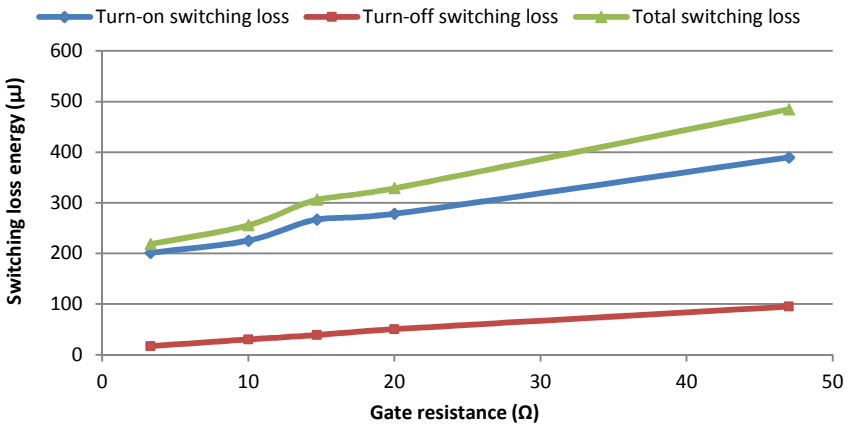



Figure 4.18 Switching energy losses as a function of gate resistance (experimental)

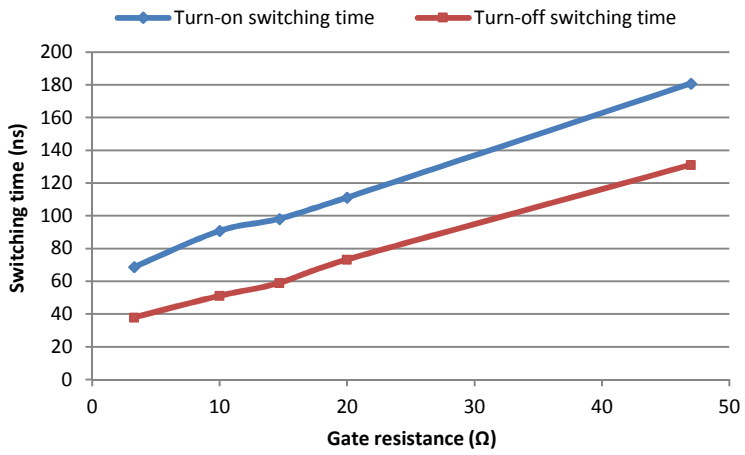



Figure 4.19 Switching times as a function of gate resistance (experimental)

The measured losses (solid line) in experiments as a function of load current are compared to model predicted losses (dashed line) in Fig 4.20. The measured losses (solid line) in experiments as a function of gate resistance are compared to model predicted losses (dashed line) in Fig 4.21. Good agreement is achieved between the losses calculated by the proposed model and the measured losses.

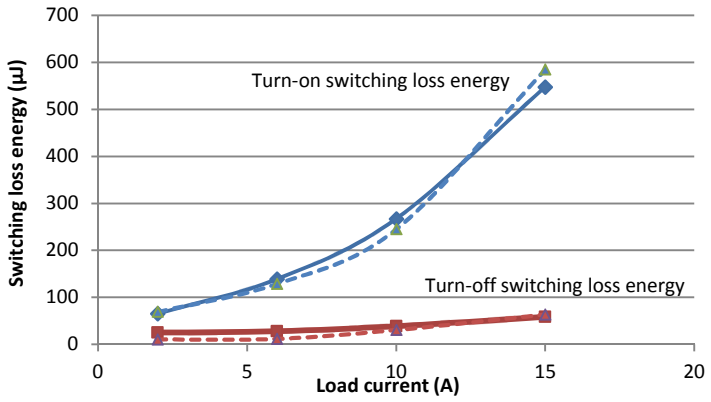



Figure 4.20 Comparison of SiC MOSFET switching losses as a function of load current

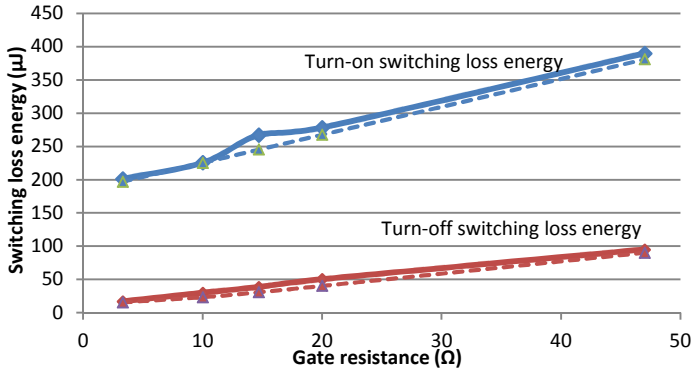



Figure 4.21 Comparison of SiC MOSFET switching losses as a function of gate resistance

Fig 4.22 shows the comparison of SiC MOSFET switching losses at 10A load current for various gate resistance values calculated in three different ways: losses obtained from experimental measurement, losses obtained from the proposed model, and losses obtained from the conventional model (piecewise linear model). The conventional loss model does not consider parasitic inductances and device nonlinear capacitances [68]. It is noted that the conventional model predicts the switching loss with significant errors in all cases. Specifically, the conventional method underestimates the actual switching loss for SiC MOSFET. In Fig 4.23, the same comparison of SiC MOSFET switching losses is shown for various values of load currents, when the gate resistance is

14.7Ω. Similarly, the conventional loss model does a poor job in predicting the total switching loss. In particular, the error of conventional model predicted results becomes more significant as the inductive load current increases. At load current $I_o$=15A, the measured switching loss is 606.25μJ, while the predicted switching loss based on conventional loss model is only 341.32μJ.

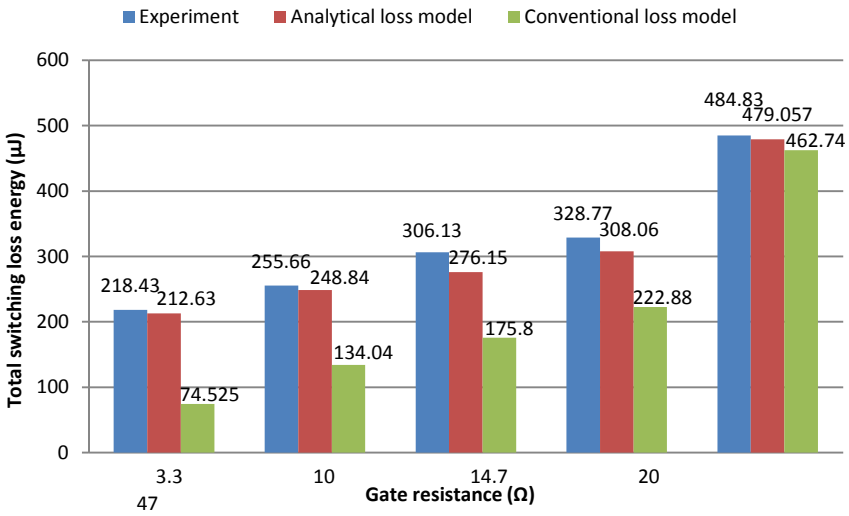



Figure 4.22 Comparison of SiC MOSFET switching losses as a function of gate resistance

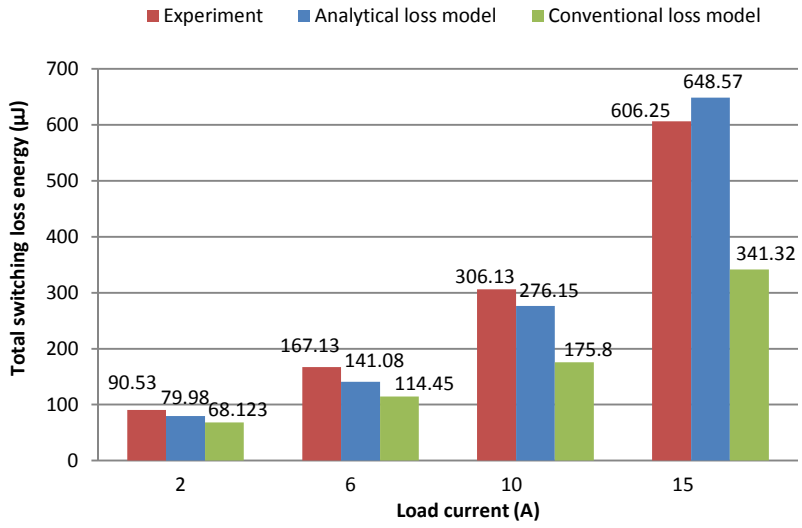



Figure 4.23 Comparison of SiC MOSFET switching losses as a function of load current

## 4.3 DISCUSSION

### 4.3.1 ACTUAL SWITCHING LOSSES VERSUS MEASURED SWITCHING LOSSES

The accurate method to calculate the switch loss of MOSFET is to calculate the overlap between the channel current $I_{ch}$ and drain-source voltage $V_{ds}$. However, the practical method to measure the switching loss of MOSFET is to calculate the overlap between the drain current $I_{ds}$ and drain-source voltage $V_{ds}$, because the MOSFET channel current is usually not accessible to be measured. As shown in Fig 4.24, the MOSFET capacitances $C_{gd}$ and $C_{ds}$ tend to make the measured drain current $I_{ds}$ outside of MOSFET deviate from the channel current $I_{ch}$, when drain-source voltage $V_{ds}$ rises or drops.

During the turn-on transition, the $C_{gd}$ and $C_{ds}$ discharging currents make $I_{ch}>I_{ds}$, therefore, the real turn-on switching loss is larger than the measured one. In contrast, in the turn-off transition, the $C_{gd}$ and $C_{ds}$ charging currents make $I_{ch}<I_{ds}$, and the real turn-off switching loss is smaller than the measured one. The energy stored in the output capacitance during turn-off transition is dissipated in the channel, when the MOSFET is turned on.

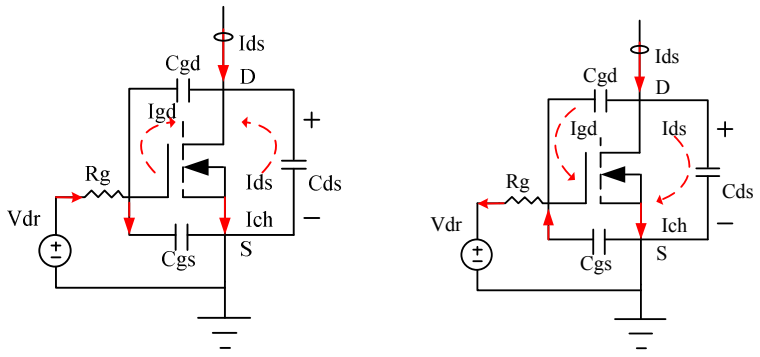



Figure 4.24 SiC MOSFET operation (a) when drain-source voltage drops (b) when drain-source voltage rises

### 4.3.2 Influence of Parasitic Inductances on Switching Losses

The analytical loss model is used to analyze the influence of main loop parasitic inductance $L_s$ and common source inductance $L_{S2}$ on switching losses. Fig 4.25 shows the calculated turn-on and turn-off switching loss energies with different main loop inductances ($L_s$) for inductive load switching at 500V input, 10A load current, and 14.7Ω gate resistance. With the increase of $L_s$, the turn-on switching loss energy decreases, because the inductive voltage drop of $V_{ds}$ in period [$t_1$, $t_2$] increases. With the increase of $L_s$, the turn-off loss increases, mainly because of a larger voltage overshoot of $V_{ds}$ and a slower decrease of $I_{ds}$ in period [$t_9$, $t_{10}$]. Another way to explain the effect of $L_s$ is to say that it acts as a turn-on snubber, decreasing turn-on losses but increasing turn-off losses. Fig 4.26 shows the calculated turn-on and turn-off switching loss energies with different common source inductances ($L_{s2}$) for inductive load switching at 500V input, 10A load current, and 14.7Ω gate resistance. Both turn-on and turn-off switching loss energies increase with the increase of $L_{s2}$, due to the smaller rate of $I_{ds}$ and longer duration in periods [$t_1$, $t_2$] and [$t_9$, $t_{10}$]. It can be said that inductance Ls2 introduces a negative

feedback from MOSFET current to the gate driver that slows down both MOSFET turn-on and MOSFET turn-off, increasing losses.

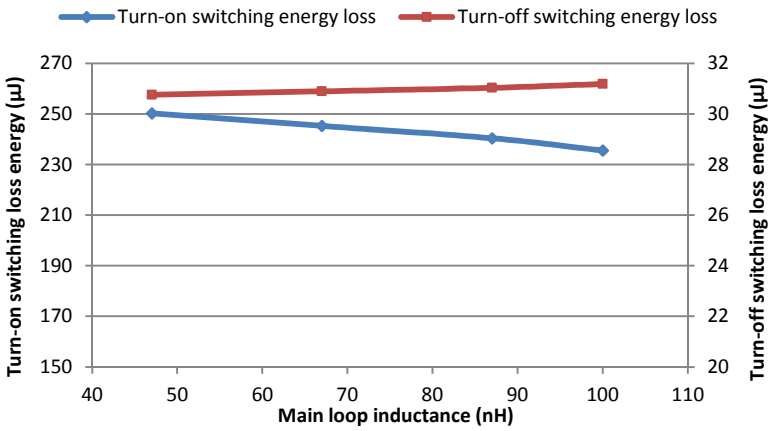



Figure 4.25 Turn-on and turn-off switching energy losses under the influence of main loop parasitic inductance

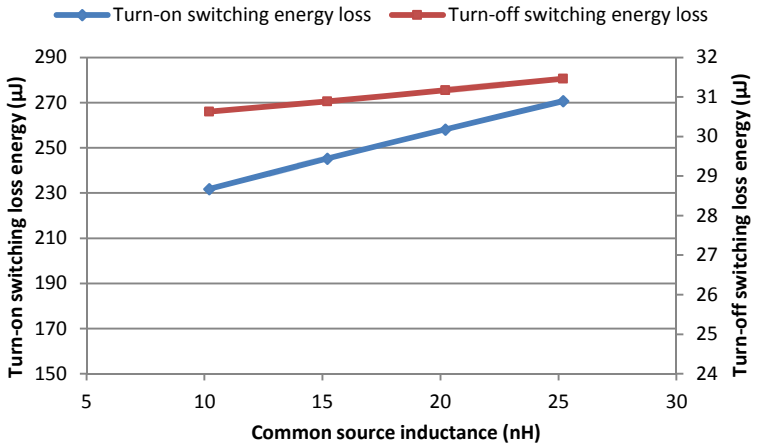



Figure 4.26 Turn-on and turn-off switching energy losses under the influence of common source parasitic inductance

## 4.4 SUMMARY

A simple and accurate analytical loss model for SiC power devies is developed. This model takes into account device nonlinear capacitances and parasitic inductances in the circuit, which is a very important feature for circuit designers. In addition, the ringing

loss and the loss from reverse capacitive charging current of SiC Schottky diode are considered. The turn-off and turn-on transitions are analyzed in detail. Two different operation modes are derived for the turn-off transition. The proposed model is validated by numerous experimental results, and the accuracy comparison of the proposed analytical loss model and conventional piecewise linear loss model is presented. The difference between real switching losses and measured switching losses is discussed, and the influence of the parasitic inductances on switching losses is demonstrated.

# CHAPTER 5

# PERFORMANCE PROJECTION AND SCALABLE LOSS MODEL OF SIC MOSFETS AND SIC SCHOTTKY DIODES

## 5.1 INTRODUCTION

Power semiconductor devices realized using wide bandgap semiconductor materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), provide better performance than traditional silicon (Si) power devices. SiC is one of the most promising semiconductor materials for high-voltage, high-speed and low-loss power switching applications, due to its superior physical characteristics, such as wider band-gap (3 times higher than Si), higher thermal conductivity, and higher critical breakdown electric field.

SiC power MOSFET is a very good candidate for high-switching-frequency and low-loss power conversion applications. The lower on-resistance makes SiC power MOSFETs an ideal choice in high power applications, offering similar conduction loss as Si IGBTs while operating at a much higher switching frequency. The switching loss of a SiC power MOSFET is much lower than that of a Si IGBT or Si GTO for the same voltage and current ratings, due to its lower device capacitance. In 2011, Cree launched industry's first commercial SiC power MOSFET, which provided blocking voltage up to 1200V with an 80mΩ on-resistance at room temperature. Presently, the n-channel 1200V SiC power MOSFET commercial products shown in Table 5-1 are available from Cree [69]. Other power semiconductor manufacturers are now offering similar products in the

market. Data from product datasheets can be used to parameterize device loss models that can be used to evaluate device in-circuit performance. Cree and other semiconductor manufacturers are also evaluating SiC power MOSFETs with higher blocking voltages (>1.2kV). However, higher-voltage SiC MOSFETs (>1.7kV) are not commercially available at the present time. Consequently no datasheet data is available and only limited sample characterization has been published in the literature. In order to analyze the device behavior of upcoming high-voltage SiC MOSFETs (>1.7kV), power electronics researchers and engineers have a need for methods for future device performance projection.

The Schottky diode is also a very attractive unipolar device, formed by an electrically non-linear contact between a metal and a semiconductor bulk region. Cree has recently introduced its SiC Schottky diode products, with rated voltage ranging from 600V to 1700V, and rated current ranging from 1A to 100A. SiC Schottky diode is a very promising candidate to replace in the future silicon p-i-n diode for blocking voltage range from 600V to 3000V. Performance projection of SiC Schottky diodes for higher voltage and higher current ratings are also of interest for power electronics engineers.

This chapter proposes a performance projection method and a scalable loss model for SiC MOSFETs and SiC Schottky diodes. To my knowledge, this is the first scalable loss model that provides performance projection capability for future SiC MOSFETs and SiC Schottky diodes in the literature. The parameters of these models are extracted from device datasheets by using a curve fitting method. Loss estimation of future SiC MOSFETs and SiC Schottky diodes can be performed based on the proposed scalable loss model.

Table 5.1 Current status of mature SiC MOSFETs from Cree

| Packaged device part number | Bare die part number | $V_{(BR)DSS}$ | $I_D$ | $R_{DS(on)}$ | $A_{chip}$ | $R_{th}$ | $Q_{gd}$(800 V) |
|---|---|---|---|---|---|---|---|
| C2M0160120D | CPM2-1200-0160B | 1200V | 19 A | 160mΩ | 6.2857mm$^2$ | 0.9K/W | 14nC |
| C2M0080120D | CPM2-1200-0080B | 1200V | 36 A | 80mΩ | 10.416mm$^2$ | 0.6K/W | 23nC |
| C2M0040120D | CPM2-1200-0040B | 1200V | 60 A | 40mΩ | 18.290mm$^2$ | 0.34K/W | 37nC |
| C2M0025120D | CPM2-1200-0025B | 1200V | 90 A | 25mΩ | 26.017mm$^2$ | 0.24K/W | 50nC |

## 5.2 Performance Projection Method

### 5.2.1 SiC MOSFET

Fig 5.1 shows voltage and current ratings of the commercially available SiC power MOSFETs from Cree listed in Table 5.1. For future applications, extrapolation of device characteristics to higher voltage and current ratings allows answering the following questions. How much chip area is required for a certain amount of drain current? How small a value of on-state resistance can be achieved for higher voltage (>1.7kV) SiC MOSFETs? These questions are addressed in this chapter by the development of a performance projection method for SiC MOSFETs. The performance projection method provides scaling equations as a function of current and voltage ratings for quantities like chip area, thermal resistance, gate-drain charge and on-state resistance.

1) Chip area: Assuming that the device drain current rating is proportional to its chip area, the projection equation of chip area based on drain current rating is given by:

$$A_{chip}(mm^2) = \frac{I_D(A)}{3.3925 A/mm^2} \qquad \text{Equation 5-1}$$

where $I_D(A)$ is the device drain current rating. The above projection formula is derived from the chip current density of available SiC power MOSFETs obtained from datasheets, see Fig 5.2. Notice the linear dependence of drain current rating versus chip area.

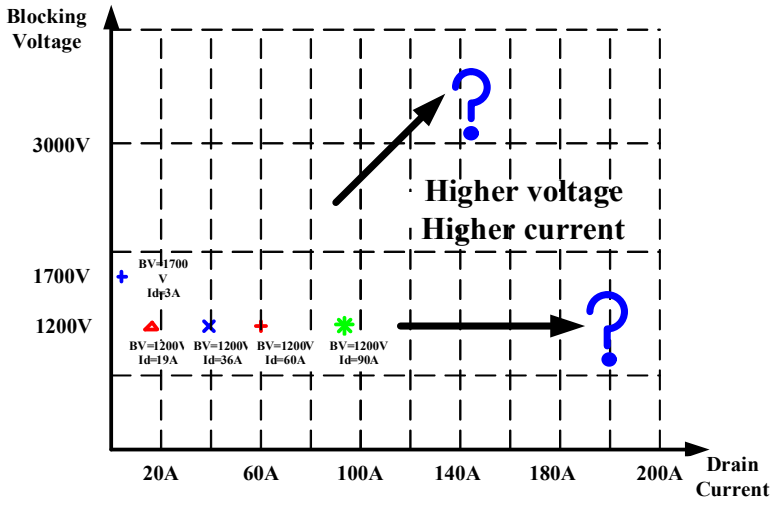



Figure 5.1 Ratings of SiC power MOSFETs available from Cree

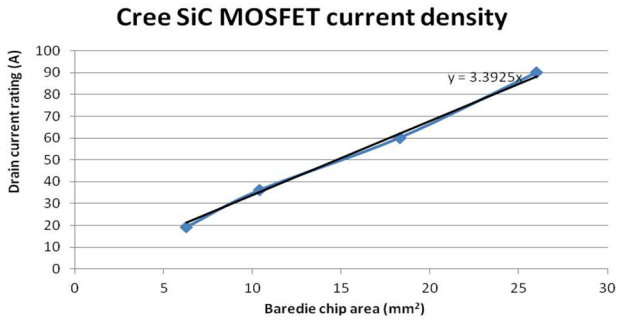



Figure 5.2 SiC power MOSFET drain current rating ($I_D$) versus chip area ($A_{chip}$)

2) Thermal resistance: The thermal resistance between junction and case for each device is plotted versus chip area in Fig 5.3. Curve fitting provides the following formula for thermal resistance $R_{th(J-C)}$ as a function of chip area. The fitting equation for thermal resistance versus chip area is given by:

$$R_{th(J-C)}(K/W) = \frac{5.4749}{A_{chip}(mm^2)} + 0.0434 \qquad \text{Equation 5-2}$$

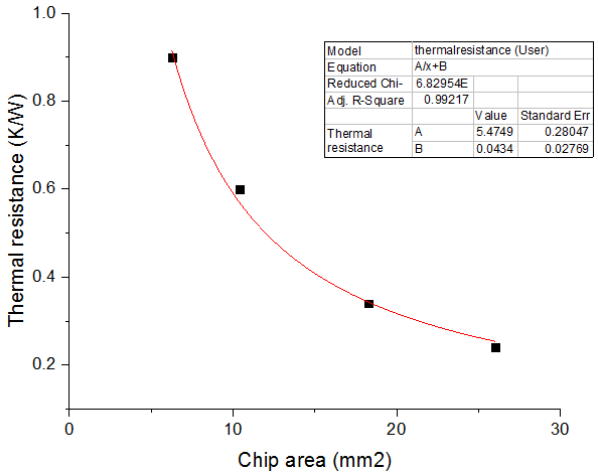



Figure 5.3 SiC power MOSFET thermal resistance ($R_{th\ (J-C)}$) versus chip area ($A_{chip}$)

3) Gate-drain charge: Fig 5.4 shows how gate-drain charge changes as a function of chip area. The projection formula of gate-drain charge based on chip area is given by:

$$Q_{gd}(nC) = A_{chip}(mm^2) \times 1.9882 \qquad \text{Equation 5-3}$$

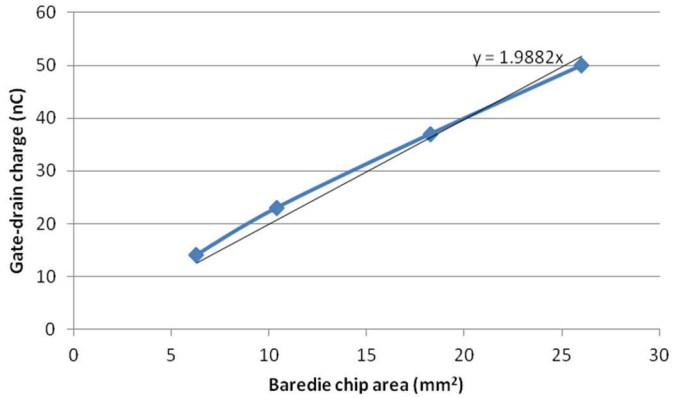



Figure 5.4 SiC power MOSFET gate-drain charge ($Q_{gd}$) versus chip area ($A_{chip}$)

Combining equations (5-1) and (5-3), the projected gate-drain charge as a function of drain current rating is found as:

$$Q_{gd}(nC) = \frac{I_D(A)}{3.3925} \times 1.9882 = 0.5861 \times I_D(A) \qquad \text{Equation 5-4}$$

4) On-state resistance: In [70], Cree provides values of specific on-state resistance for SiC power MOSFETs as a function of blocking voltage from 900V up to 15kV, as shown in Table 5.2.

Table 5.2 Specific on resistance of the SiC DMOSFETs measured at gate bias of 20V as a function of breakdown voltage at room temperature

| Blocking voltage (V) | Specific on-state resistance (mΩ.cm$^2$) |
|---|---|
| 900 | 2.3 |
| 1200 | 2.7 |
| 1700 | 3.38 |
| 3300 | 10.6 |
| 10000 | 123 |
| 15000 | 208 |

The specific on-state resistance (mΩ·cm$^2$) formula obtained from curve fitting is given by:

$$R_{on,sp} = 9.6 \times 10^{-7} V_{BD}^2 + 1.45 \qquad \text{Equation 5-5}$$

### 5.2.2 SiC Schottky Diode

This section describes the performance projection of SiC Schottky diodes based on device datasheet data.

1) Chip area: $I_F$(A) is the device forward current rating. Assuming that $I_F$(A) is proportional to diode chip area, the chip current density (=$I_F/A_{chip}$) can be obtained.

$$A_{chip}(mm^2) = \frac{I_F(A)}{8.2525 A/mm^2} \qquad \text{Equation 5-6}$$

2) Thermal resistance: The thermal resistance between junction and case for each device is a function of chip area. Curve fitting of thermal resistance $R_{th(J-C)}$ obtained from datasheets results in the following equation.

$$R_{th(J-C)}(K/W) = \frac{2.3122}{A_{chip}(mm^2)} + 0.4935 \qquad \text{Equation 5-7}$$

The projected thermal resistance as a function of forward current is obtained by combining equations (5-6) and (5-7):

$$R_{th(J-C)}(K/W) = \frac{19.0814}{I_F(A)} + 0.4935 \qquad \text{Equation 5-8}$$

3) Junction capacitance (zero voltage bias): The projection formula of junction capacitance $C_{r0}$ (zero bias voltage) based on chip area is given by:

$$C_{r0}(pF) = A_{chip}(mm^2) \times 154.88 \qquad \text{Equation 5-9}$$

Combining equations (5-6) and (5-9), the projected junction capacitance $C_{r0}$ as a function of forward current is given by (5-10).

$$C_{r0}(pF) = \frac{I_F(A)}{8.2525} \times 154.88 = 18.7676 \times I_F(A) \qquad \text{Equation 5-10}$$

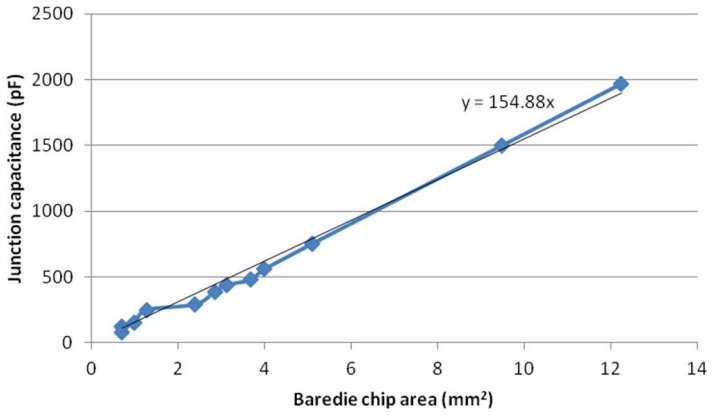



Figure 5.5 SiC power MOSFET junction capacitance ($C_{r0}$) versus chip area ($A_{chip}$)

4) On-state resistance: The specific on-state resistance ($m\Omega \cdot cm^2$) formula for SiC Schottky diodes is obtained from curve fitting:

$$R_{on,sp} = 2.72 \times 10^{-6} V_{BD}^2 + 0.43044 \quad \text{Equation 5-11}$$

5) Built-in voltage potential: The diode built-in voltage potential is assumed to be 0.935V at room temperature and it has a negative temperature coefficient.

$$V_{bi}(T_{j,D}) = 1.475 - T_{j.D} \times 1.8 \times 10^{-3} \quad \text{Equation 5-12}$$

$T_{j,D}$ is the junction temperature of SiC Schottky diode in Kelvin.

## 5.3 Scalable Loss Model

In switching converters power semiconductor devices operate in clamped inductive switching mode. Their power loss is composed of two parts: conduction loss and switching loss. The loss model is interfaced with the thermal model as shown in Fig 5.6. The electrical loading of converter (e.g. switching frequency, DC bus voltage, load current, etc.) is first translated into power loss via the device loss model. This power loss is input to the thermal impedance model, which computes the junction temperature,

which is then fed back to the loss model so that the temperature dependency of power losses can be properly accounted for.

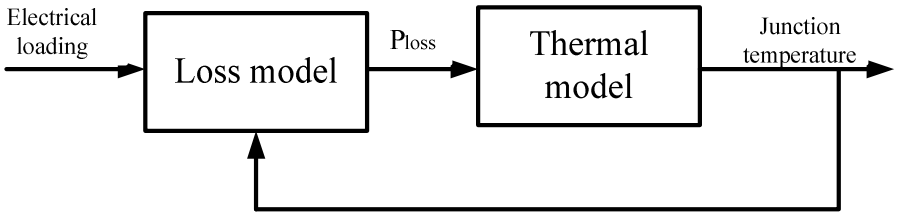



Figure 5.6 Electro-thermal model

### 5.3.1 SiC MOSFET

1) Conduction loss

The conduction loss of a SiC power MOSFET is modeled as follows:

$$P_{Cond,MOSFET} = I_{rms}^{2} R_{on,M}(T_j) \qquad \text{Equation 5-13}$$

where $I_{rms}$ is the MOSFET conduction current RMS value, and $R_{on,M}(T_j)$ is the junction-temperature-dependent MOSFET on-state resistance, and $T_j$ is the MOSFET junction temperature.

Assuming that the chip active area is 50% of the total chip area, the on-state resistance (unit: Ω) expression at room temperature is given by:

$$\begin{aligned} R_{on,M}(T_{300}) &= R_{on,sp} / (0.5 A_{chip}) \\ &= (9.6\times10^{-7} V_{BD}^{2} + 1.45)\times 200 \times 0.001 / (I_D / 3.3925) \\ &= 0.6785\times(9.6\times10^{-7} V_{BD}^{2} + 1.45) / I_D \end{aligned} \qquad \text{Equation 5-14}$$

The expression on the second line of (5-14) is obtained substituting the specific on-state resistance projection formula (5-5) obtained previously. The on-state resistance (unit: Ω) as a function of junction temperature is given by:

$$R_{on,M}(T_j) = R_{on,M}(T_{300})(\frac{T_j}{300})^{2.4}$$
$$= [0.6785 \times (9.6 \times 10^{-7} V_{BD}^2 + 1.45) / I_D](\frac{T_j}{300})^{2.4} \quad \text{Equation 5-15}$$

where $I_D(A)$ is the device drain current rating, and $V_{BD}$ is the device reverse voltage rating.

2) Switching loss

The switching loss of the power MOSFET at a given operating condition (blocking voltage $V$, and conduction current $I$) is modeled as varying linearly as a function of both V and I. Therefore

$$E_{on,M}(V,I) = E_{on,M,nom} \frac{V}{V_{nom}} \frac{I}{I_{nom}} \quad \text{Equation 5-16}$$

$$E_{off,M}(V,I) = E_{off,M,nom} \frac{V}{V_{nom}} \frac{I}{I_{nom}} \quad \text{Equation 5-17}$$

where $E_{on,M,nom}$ and $E_{off,M,nom}$ are turn-on energy loss and turn-off energy loss at nominal operating conditions (device blocking voltage $V_{nom}$, and conduction current $I_{nom}$).

The nominal values are taken from datasheet values of the latest generation of SiC power MOSFETs from Cree with parameters as listed in Table 5.3.

Table 5.3 Nominal energy loss from device datasheet

| Part number | $I_D$ | $E_{on}$ (testing voltage, testing current) | $E_{off}$ (testing voltage, testing current) |
|---|---|---|---|
| C2M0160120D | 19A | 79μJ (800V,10A) | 57μJ (800V,10A) |
| C2M0080120D | 36A | 265μJ (800V,20A) | 135μJ (800V,20A) |
| C2M0040120D | 60A | 1000μJ (800V,40A) | 400μJ (800V,40A) |

Fig 5.7 shows the nominal turn-on energy loss and nominal turn-off energy loss for SiC power MOSFETs with different chip areas. Please note that all the nominal values are normalized to the reference case ($V_{nom}$=800V, $I_{nom}$=10A).

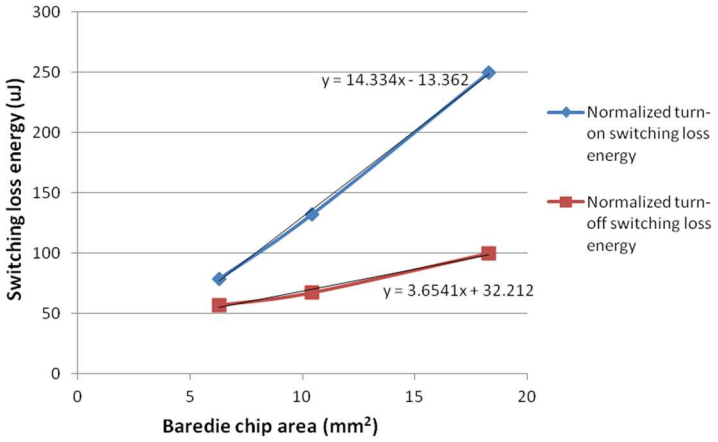



Figure 5.7 SiC MOSFET nominal turn-on loss energy and nominal turn-off loss energy versus chip area ($A_{chip}$)

Curve-fitting the nominal turn-on energy loss $E_{on,M,nom}$ of Fig 5.7 gives the expression:

$$E_{on,M,nom}(\mu J) = 14.334 A_{chip}(mm^2) - 13.362 \qquad \text{Equation 5-18}$$

The nominal turn-on energy loss can be expressed as a function of drain current rating by substituting (5-1) into (5-18).

$$E_{on,M,nom}(\mu J) = 4.2252 \times I_D(A) - 13.362 \qquad \text{Equation 5-19}$$

Repeating the same process for turn-off energy loss $E_{off,M,nom}$ gives:

$$E_{off,M,nom}(\mu J) = 3.6541 A_{chip}(mm^2) + 32.212 \qquad \text{Equation 5-20}$$

Substituting equation (5-1) into (5-20) yields:

$$E_{off,M,nom}(\mu J) = 1.0771 \times I_D(A) + 32.212 \qquad \text{Equation 5-21}$$

Combining equation (5-16) and (5-19) provides the desired scalable expression (5-22) for the turn-on switching loss. Similarly combining (5-17) and (5-21) yields equation (5-23).

$$E_{on,M}(V,I) = [4.2252 \times I_D(A) - 13.362]\frac{V}{800}\frac{I}{10} \quad \text{Equation 5-22}$$

$$E_{off,M}(V,I) = [1.0771 \times I_D(A) + 32.212]\frac{V}{800}\frac{I}{10} \quad \text{Equation 5-23}$$

In these equations $V$ is the MOSFET blocking voltage when it is off, and $I$ is the MOSFET conduction current when it is on, and $I_D(A)$ is the MOSFET conduction current rating.

The total loss model of a SiC power MOSFET can be calculated as:

$$\begin{aligned} P_{loss}(V,I) &= P_{Cond,loss} + P_{Sw,loss} \\ &= I_{rms}{}^2 R_{on,M}(T_j) + f_{sw}(E_{on,M} + E_{off,M}) \end{aligned} \quad \text{Equation 5-24}$$

Substituting equations (5-13), (5-22) and (5-23) into (5-24), the total power loss equation (5-25) (unit: J) is obtained.

$$\begin{aligned} & P_{loss}(V,I) = I_{rms}{}^2 R_{on,M}(T_j) + f_{sw}(E_{on,M} + E_{off,M})/1000000 \\ & = I_{rms}{}^2[0.6785 \times (9.6 \times 10^{-7} V_{BD}^2 + 1.45)/I_D](\frac{T_j}{300})^{2.4} \\ & + f_{sw}([4.2252 \times I_D - 13.362]\frac{V}{800}\frac{I}{10} + [1.0771 \times I_D + 32.212]\frac{V}{800}\frac{I}{10})/1000000 \\ & = I_{rms}{}^2[0.6785 \times (9.6 \times 10^{-7} V_{BD}^2 + 1.45)/I_D](\frac{T_j}{300})^{2.4} + f_{sw}\frac{VI}{8 \times 10^9}[5.3023 \times I_D + 18.85] \end{aligned} \quad \text{Equation 5-25}$$

where $f_{sw}$ is the switching frequency.

In steady state, the following equation describes the thermal model:

$$T_j - T_{amb} = P_{loss}(V,I) \times (R_{th(J-C)} + R_{th(C-S)} + R_{th(S-A)}) \quad \text{Equation 5-26}$$

where $T_j$ is the junction temperature of the SiC MOSFET, $T_{amb}$ is the ambient temperature, $R_{th(J-C)}$ is the thermal resistance from device junction to case, $R_{th(C-S)}$ is the thermal resistance from case to heatsink, and $R_{th(S-A)}$ is the thermal resistance from heatsink to ambient.

### 5.3.2 SiC Schottky Diode

1) Conduction loss

The conduction loss of a SiC power Schottky diode is modeled as follows:

$$P_{Cond,Diode} = I_{d\_rms}{}^2 R_{on,D}(T_{j,D}) + V_{bi}(T_{j,D}) I_{d\_ave} \qquad \text{Equation 5-27}$$

where $I_{d\_rms}$ is the diode conduction current RMS value, $I_{d\_ave}$ is the diode conduction current average value, and $R_{on,D(Tj,D)}$ is the junction temperature dependent diode on-state series resistance. $T_{j,D}$ is the junction temperature of this SiC power Schottky diode. $V_{bi(Tj,D)}$ is the junction temperature dependent diode built-in voltage potential, which is given by equation (5-12).

Assuming that the chip active area is 50% of the total chip area, based on the specific on-state resistance projection formula (5-11) described above, the on-state resistance (unit: Ω) expression at room temperature is given by:

$$\begin{aligned} R_{on,D}(T_{300}) &= R_{on,sp} / (0.5 A_{chip}) \\ &= (2.72\times10^{-6} V_{BD}^2 + 0.43044)\times 0.2 / (I_F / 8.2525) \\ &= 1.65\times(2.72\times10^{-6} V_{BD}^2 + 0.43044) / I_F \end{aligned} \qquad \text{Equation 5-28}$$

where $V_{BD}$ is the device breakdown voltage and $I_F$ is the forward current rating of the SiC power Schottky diode.

The on-state series resistance (unit: Ω) as a function of junction temperature for power Schottky diodes is given by:

$$\begin{aligned} R_{on,D}(T_{j,D}) &= R_{on,D}(T_{300})\left(\frac{T_{j,D}}{300}\right)^{2.4} \\ &= [1.65\times(2.72\times10^{-6} V_{BD}^2 + 0.43044) / I_F]\left(\frac{T_{j,D}}{300}\right)^{2.4} \end{aligned} \qquad \text{Equation 5-29}$$

2) Switching loss

For inductive switching operation in a power converter, typically SiC Schottky diode switching losses are negligible in comparison with SiC MOSFET switching losses and therefore will not be considered.

The total loss model of a SiC power Schottky diode can be calculated as:

$$P_{loss,D}(V,I) = P_{Cond,Diode} + P_{Sw,Diode} = I_{d\_rms}{}^2 R_{on,D}(T_{j,D}) + V_{bi}(T_{j,D}) I_{d\_ave}$$
$$= I_{d\_rms}{}^2 [1.65 \times (2.72 \times 10^{-6} V_{BD}^2 + 0.43044) / I_F] (\frac{T_{j,D}}{300})^{2.4} + (0.98 - T_{j.D} \times 1.8 \times 10^{-3}) I_{d\_ave} \quad \text{Equation 5-30}$$

where $f_{sw}$ is the switching frequency.

In steady state, the following equation describes the thermal model:

$$T_{j,D} - T_{amb} = P_{loss,D}(V,I) \times (R_{th(J-C)} + R_{th(C-S)} + R_{th(S-A)}) \quad \text{Equation 5-31}$$

where $T_{j,D}$ is the junction temperature of the SiC Schottky diode. $T_{amb}$ is the ambient temperature, $R_{th(J-C)}$ is the thermal resistance from device junction to case, $R_{th(C-S)}$ is the thermal resistance from case to heatsink, and $R_{th(S-A)}$ is the thermal resistance from heatsink to ambient.

## 5.4 Loss Analysis of a SiC Boost Converter

In this section, the loss models of the SiC MOSFET and SiC Schottky diode are used to calculate device conduction and switching losses in a high frequency DC-DC converter, in order to study how these losses affect the overall performance of the conversion system. A simple hard-switching DC-DC boost converter is selected in this work to perform the investigation in this section. The main specifications of this SiC DC-DC boost converter are summarized in Table 5.4.

. Table 5.4 Specifications of a SiC DC-DC boost converter

| | |
|---|---|
| Output Voltage | 1000V |
| Nominal output power | 20kW |
| Duty cycle | 0.5 |
| Ambient temperature | 25 ºC |
| Junction temperature limitation | 150 ºC |
| Thermal resistance (from case to heatsink) | 2K/W |
| Heatsink thermal resistance | 0.1K/W |

Typically, selecting device current rating (proportional to chip area) involves a tradeoff between conduction and switching losses. If devices with larger current ratings are selected, the related conduction losses are lower, and switching losses are higher. Conversely, devices with lower current ratings result in higher conduction losses and lower switching losses.

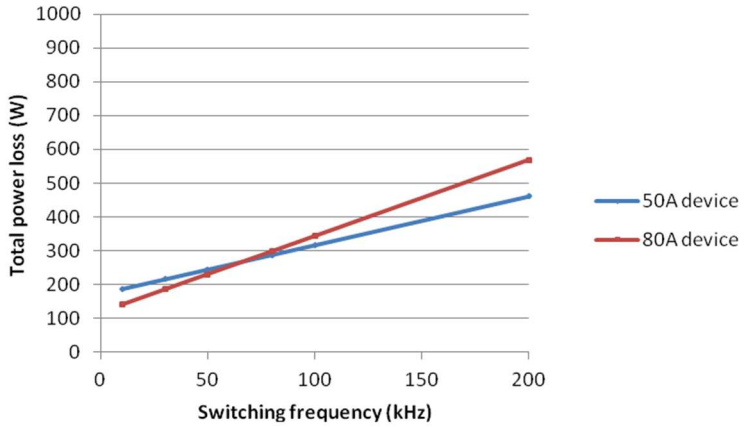



Figure 5.8 Total power loss of SiC boost converter at full power as a function of switching frequency for two different device current ratings

As shown in Fig 5.8, as frequency increases from 10 kHz to 200 kHz, the power loss of the SiC converter at rated output power linearly increases due to increasing switching losses. It can be seen that the 80A devices have lower power loss at lower

switching frequencies, whereas the 50A devices have lower power loss at higher switching frequencies. The cross point is about 70 kHz. This is due to the fact that devices with higher current ratings (in proportion to chip area) have lower on-state resistances and higher device capacitances, while devices with lower current ratings have higher on-state resistance and lower device capacitance.

The loss distribution of the SiC boost DC-DC converter is shown in Fig 5.9, at full output power, and 100 kHz switching frequency. The figure clearly shows that the MOSFET switching loss dominates the total MOSFET losses.

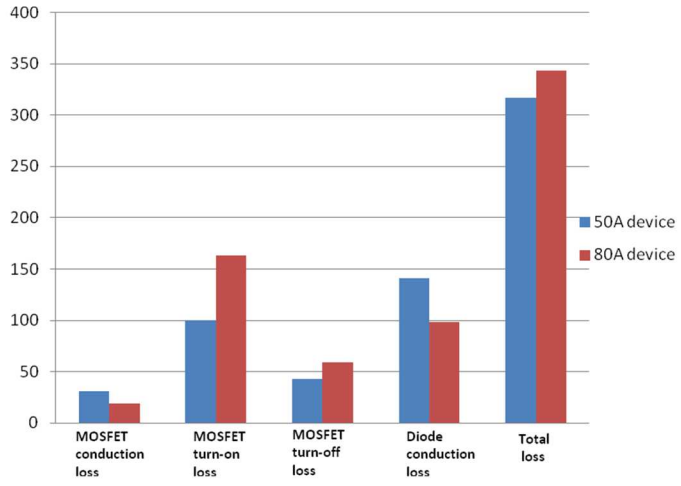



Figure 5.9 Power loss breakdown of SiC boost converter at full power rating and switching frequency 100kHz

Fig 5.10 illustrates the efficiency of the SiC converter at different junction temperatures (from 25 ºC to 125 ºC). Note that only semiconductor device losses are considered. The efficiency decreases as temperature increases due to increased conduction losses. Moreover, the SiC converter with 50A devices has higher efficiency than the converter with 80A devices, at lower junction temperatures. The opposite is true at higher junction temperatures.

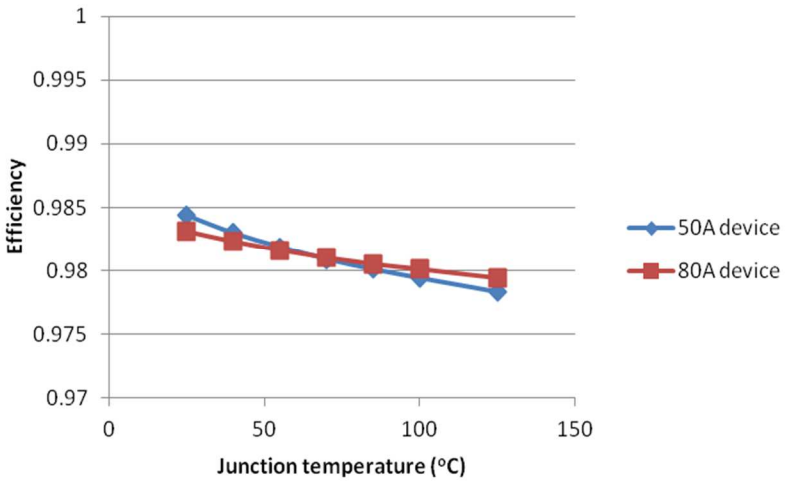



Figure 5.10 Efficiency of SiC boost converter at full power (20 kW), switching frequency 100 kHz as a function of junction temperature

Fig 5.11 shows the calculated losses based on the scalable loss model, as the device chip areas (current ratings) increase. As the chip areas increase, the device conduction losses decrease, and the device switching losses increase. The optimum chip area (MOSFET chip area plus diode chip area) is about 30~35 $mm^2$.

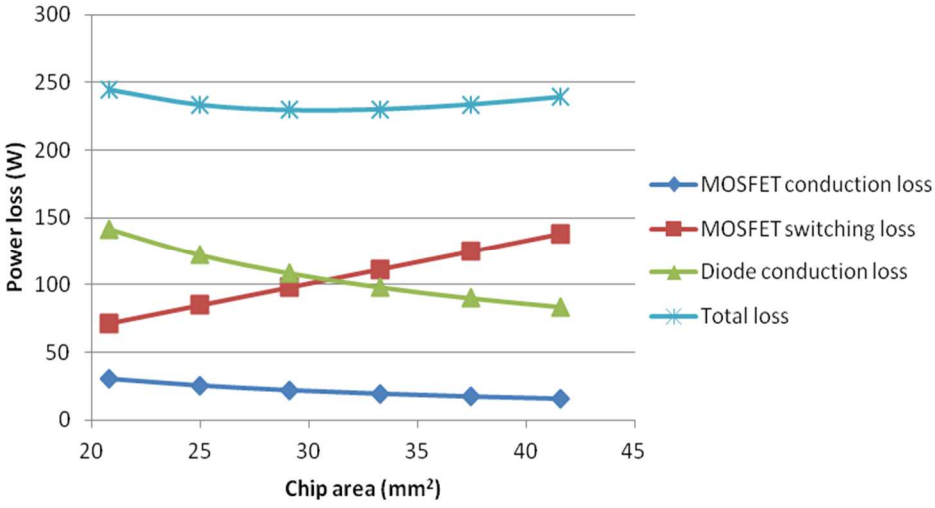



Figure 5.11 Power loss distribution of SiC boost converter at full power rating 20 kW, switching frequency 50 kHz with different chip areas

## 5.5 SUMMARY

In this chapter, a simple behavioral projection method for future SiC MOSFETs and SiC Schottky diodes is developed, and a scalable loss model for future SiC MOSFETs and SiC Schottky diodes is proposed. The loss model parameters are extracted from device datasheets by using a curve fitting method. The formulas so obtained can be used to calculate device parameters, such as chip area, thermal resistance, gate-drain charge, junction capacitance and on-resistance, as a function of device voltage and current ratings. Parameter values can be projected for future SiC power devices having higher voltage and higher current ratings. Loss estimation for future SiC MOSFETs and SiC Schottky diodes can be performed using the proposed scalable loss model. The scalable loss model is demonstrated in the loss analysis of a SiC boost DC-DC converter.

# CHAPTER 6

# CONCLUSIONS AND FUTURE WORK

## 6.1 CONCLUSIONS

This dissertation discusses the device modeling and loss analysis of wide bandgap power semiconductor devices. Three wide bandgap power semiconductor devices are studied: GaN HEMT, SiC MOSFET and SiC Schottky diode. The basic objective in device modeling is to obtain the functional relationship among the electrical and thermal variables of the devices that are to be modeled. Loss models use closed form mathematical equations to accurately describe power loss mechanisms and quantify losses as a function of various design parameters.

First, a simple physics-based model for GaN HEMT including both forward and reverse channel current conduction is proposed and validated under both static and switching conditions. Static characterization is done using a curve tracer and C-V analyzer. For dynamic switching characterization, a Double Pulse Tester (DPT) printed circuit board (PCB) with both a resistive load and an inductive load is built. The 3-D inductance extraction software program FastHenry is used to estimate the parasitic inductances from DPT circuit PCB layout. The extracted gate driving loop and drain-to-source main switching loop parasitic inductances from the PCB layout are used in Pspice simulation circuit together with the developed GaN HEMT model to accurately simulate the resistive and inductive switching transient behavior of the power devices.

Second, to utilize the SiC MOSFET body diode in power converters, the static and switching behavior of SiC MOSFET body diode is characterized and analyzed. The static characteristics of SiC MOSFET body diode are measured at varied junction temperatures. The dynamic characteristics of SiC MOSFET body diode are tested based on Double Pulse Tester (DPT) under different current commutating slopes, forward conduction currents and junction temperatures. A diode model is introduced, which uses a Fourier Series solution for the ambipolar diffusion equation in the drift region. The parameter extraction procedure is described. The diode model using the parameters extracted demonstrates good agreement with experimental results.

Third, a simple and accurate analytical loss model for SiC power devices is proposed. A novel feature of this loss model is that it considers the package and PCB parasitic elements in the circuits, nonlinearity of device junction capacitance and ringing loss. The proposed model identifies the switching waveform subintervals, and develops the analytical equations in each switching subinterval to calculate the switching loss. Inductive turn-on and turn-off are thoroughly analyzed. A double pulse test-bench is built to characterize inductive switching behavior of the SiC devices. The analytical results are compared with experimental results. The results show that the proposed loss model can predict switching loss more accurately than the conventional loss model.

Finally, a simple behavioral projection method for future SiC MOSFETs and SiC Schottky diodes is developed, and a scalable loss model for future SiC MOSFETs and SiC Schottky diodes is proposed. The performance projection method provides estimated parameters also for upcoming devices with higher power ratings than currently commercially available. These parameters are used in the scalable loss models to estimate

power losses. The performance projection and scalable loss model are established based on data from Cree's product datasheets. The loss breakdown analysis of a SiC DC-DC boost converter is presented to demonstrate the proposed performance projection method and scalable loss model.

## 6.2 Future Work

Based on the research results presented in this dissertation, future work can be carried out as follows:

1) Development of the analytical loss model for a SiC phase leg configuration

In order to extend the proposed analytical loss to more converter topologies, such as inverter, half bridges, full bridges and so on, an analytical loss model for a SiC phase leg configuration can be investigated [71][72][73].

The nonlinearity of device capacitances and the parasitic inductances in the circuit, such as the source inductance shared by the power stage and gate driver loop, the drain inductance, etc., should be considered in the loss model. In addition, the model should take into account the reverse recovery characteristics of the body diode of the SiC MOSFET, if an external anti-parallel SiC Schottky diode is not used [74].

2) Design of a SiC DC-DC buck converter

In order to demonstrate the SiC MOSFET performance and validate the proposed loss models, a DC-DC buck reference design using 1200V SiC MOSFET and 1200V SiC Schottky diode will be demonstrated. The efficiency of the power converter will be measured, and device chip temperature will be monitored during steady-state operation. The comparison of experiment, Pspice simulation, analytical loss model calculation and

scalable loss model calculation will be done, in terms of device losses and converter efficiency.

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